

NOTES04 ADDENDA

When binary encoded state assignment is used for this machine, the design equations are as below.

$$z = \text{sreg_1.Q} * \text{sreg_0.Q}$$

$$\text{sreg_1.D} = \text{/sreg_1.Q} * \text{sreg_0.Q} * \text{xx} + \text{sreg_1.Q} * \text{/sreg_0.Q}$$

$$\text{sreg_0.D} = \text{sreg_1.Q} * \text{/sreg_0.Q} * \text{/xx} + \text{/sreg_1.Q} * \text{/sreg_0.Q} * \text{xx} \\ + \text{sreg_1.Q} * \text{sreg_0.Q} * \text{xx}$$

First, Mapping these on the K-maps below we get the following

sreg_1				sreg_0		
sr1, sr0	xx= 0	xx= 1		sr1, sr0	xx= 0	xx= 1
a= 00	0	0		a= 00	0	1
b= 01	0	1		b= 01	0	0
d= 11	0	0		d= 11	0	1
c= 10	1	1		c= 10	1	0

Putting this into a state transition table gives the following.

STATE TABLE	Next State		Output
present state	xx= 0	xx= 1	Z
a= 00	a= 00	b= 01	0
b= 01	a= 00	c= 10	0
c= 10	d= 11	c= 10	0
d= 11	a= 00	b= 01	1

This then agrees with the state diagram which we started with (shown again to the right). So we have gone around in a circle - synthesis and analysis.

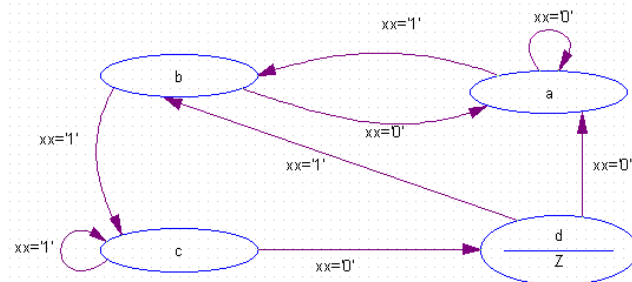


FIGURE E9-3