

## THE RAILROAD PROBLEM REVISITED

In the last notes we obtained a solution to the railroad problem, using some CPLD (which one was not specified in the notes. The solution worked but was not practical. This is a short note detailing a practical solution.

The two things that require changing (directly) are the device used (a 22V10 is sufficient - more than sufficient) and we have not accounted for the fact that the inputs are active low. One additional change is needed if the device is to be fitted into a 22V10. A binary state assignment is needed rather than the one-hot assignment in order to conserve space in the 22V10.

So, first, StateCAD was used to regenerate the VHDL module with the different state assignment (same diagram). The result is below.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY GCR01 IS
    PORT (CLK, BLK, GCR: IN std_logic;
          BELL : OUT std_logic;
          sreg : BUFFER std_logic_vector (1 DOWNTO 0));
END;

ARCHITECTURE BEHAVIOR OF GCR01 IS
    SIGNAL next_sreg : std_logic_vector (1 DOWNTO 0);
    CONSTANT AT_CROSSING : std_logic_vector (1 DOWNTO 0) := "00";
    CONSTANT IN_BLOCK : std_logic_vector (1 DOWNTO 0) := "01";
    CONSTANT NO_TRAIN : std_logic_vector (1 DOWNTO 0) := "10";
    CONSTANT PAST_CROSSING : std_logic_vector (1 DOWNTO 0) := "11";
BEGIN
    PROCESS (CLK, next_sreg)
    BEGIN
        IF CLK='1' AND CLK'event THEN
            sreg <= next_sreg;
        END IF;
    END PROCESS;

    PROCESS (sreg, BLK, GCR)
    BEGIN
        BELL <= '0';
        next_sreg<=AT_CROSSING;
        CASE sreg IS
            WHEN AT_CROSSING =>
                BELL<='1';
                IF ( GCR='0' ) THEN
                    next_sreg<=PAST_CROSSING;
                ELSE
                    next_sreg<=AT_CROSSING;
                END IF;
            WHEN IN_BLOCK =>
                BELL<='1';
                IF ( BLK='1' AND GCR='0' ) THEN
                    next_sreg<=IN_BLOCK;
                END IF;
                IF ( BLK='0' ) THEN
                    next_sreg<=NO_TRAIN;
                END IF;
                IF ( BLK='1' AND GCR='1' ) THEN
```

```

        next_sreg<=AT_CROSSING;
    END IF;
WHEN NO_TRAIN =>
    BELL<='0';
    IF ( BLK='1' ) THEN
        next_sreg<=IN_BLOCK;
    ELSE
        next_sreg<=NO_TRAIN;
    END IF;
WHEN PAST_CROSSING =>
    BELL<='0';
    IF ( GCR='0' AND BLK='1' ) THEN
        next_sreg<=PAST_CROSSING;
    END IF;
    IF ( BLK='1' AND GCR='1' ) THEN
        next_sreg<=AT_CROSSING;
    END IF;
    IF ( BLK='0' ) THEN
        next_sreg<=NO_TRAIN;
    END IF;
WHEN OTHERS =>
    END CASE;
END PROCESS;
END BEHAVIOR;

```

We shall not comment on the listing. By now you should be able to figure it out. The main module is then modified slightly.

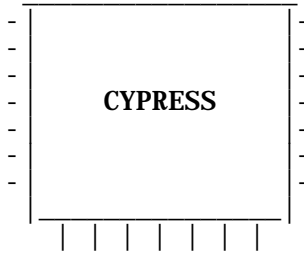
```

library ieee;
USE ieee.std_logic_1164.all;
USE work.all;
ENTITY two_track is
    PORT(
        blk1, blk2, gcr1, gcr2, clk: in std_logic;
        bellout, arm: out std_logic
    );
end two_track;
ARCHITECTURE main of two_track is
    signal bell1, bell2: std_logic;
begin
    west: Gcr01 port map (clk, not blk1, not gcr1, bell1);
    east: Gcr01 port map (clk, not blk2, not gcr2, bell2);
    bellout<=bell1 or bell2;
    process(clk)
    begin
        if (clk'event and clk='1') then
            if (bell1='1' or bell2='1') then arm<='1'; else arm<='0';
            end if;
        end if;
    end process;
end;

```

The two lines which have been changed are in bold type. First, the u1 and u2 have been replaced with more descriptive names. More important, the four track inputs have been entered as NOT values (i.e., inverted). The report obtained from this is as follows. This time we shall include the entire report (edited some to save some space). Comments on this report will be made in class.

| | | | | | |



Warp VHDL Synthesis Compiler: Version 4 IR x77  
 Copyright (C) 1991, 1992, 1993,  
 1994, 1995, 1996, 1997 Cypress Semiconductor

```
=====  

Compiling:  gcr02.vhd  

Options:    -q -yv2 -e10 -w100 -o1 -yga -fP -v10 -dc22v10 -pPALCE22V10-5PC  

gcr02.vhd  

=====
```

```
f:\warp\bin\vhdlfe.exe V4 IR x77:  VHDL parser  

Thu Oct 23 20:11:15 1997  

Library 'work' => directory 'lc22v10'  

Linking 'f:\warp\lib\common\work\cypress.vif'.  

Library 'ieee' => directory 'f:\warp\lib\ieee\work'  

Linking 'f:\warp\lib\ieee\work\stdlogic.vif'.  

Linking 'F:\fsm02h\lc22v10\gcr01.vif'.
```

f:\warp\bin\vhdlfe.exe: No errors.

```
f:\warp\bin\tovif.exe V4 IR x77:  High-level synthesis  

Thu Oct 23 20:11:17 1997  

Linking 'f:\warp\lib\common\work\cypress.vif'.  

Linking 'f:\warp\lib\ieee\work\stdlogic.vif'.  

Linking 'F:\fsm02h\lc22v10\gcr01.vif'.  

Note: Removing wires from arch. 'main' of entity 'two_track'.
```

f:\warp\bin\tovif.exe: No errors.

```
f:\warp\bin\topld.exe V4 IR x77:  Synthesis and optimization  

Thu Oct 23 20:11:19 1997  

Linking 'f:\warp\lib\common\work\cypress.vif'.  

Linking 'f:\warp\lib\ieee\work\stdlogic.vif'.  

Linking 'F:\fsm02h\lc22v10\gcr01.vif'.  

Linking 'f:\warp\lib\lc22v10\stdlogic\c22v10.vif'.
```

-----  
Detecting unused logic.  
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#### Alias Detection

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Aliasing armD to bellout  

Removing Lhs of wire blk1_not_0[7] = blk1[0]  

Removing Lhs of wire gcr1_not_1[8] = gcr1[2]  

Removing Lhs of wire blk2_not_2[14] = blk2[1]  

Removing Lhs of wire gcr2_not_3[15] = gcr2[3]  

Removing Lhs of wire armD[21] = bellout[5]  

Removing Lhs of wire west_sreg_1D[22] = west_next_sreg_1[10]  

Removing Lhs of wire west_sreg_0D[23] = west_next_sreg_0[12]  

Removing Lhs of wire east_sreg_1D[24] = east_next_sreg_1[17]  

Removing Lhs of wire east_sreg_0D[25] = east_next_sreg_0[19]  

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```

Aliased 0 equations, 9 wires.  
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Circuit simplification

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Substituting virtuals - pass 1:  
Note: Virtual equation for 'bell1' has been expanded (cost = 0):  
bell1 <= (not west\_sreg\_1);  
Note: Virtual equation for 'bell2' has been expanded (cost = 0):  
bell2 <= (not east\_sreg\_1);

Substituting virtuals - pass 2:

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Circuit simplification results:  
Expanded 2 signals.  
Turned 0 signals into soft nodes.  
Maximum expansion cost was set at 10.

-----  
Created 26 PLD nodes.  
Note: Removed unneeded node 'blk1\_not\_0'.  
Note: Removed unneeded node 'gcr1\_not\_1'.  
Note: Removed unneeded node 'bell1'.  
Note: Removed unneeded node 'blk2\_not\_2'.  
Note: Removed unneeded node 'gcr2\_not\_3'.  
Note: Removed unneeded node 'bell2'.  
Note: Removed unneeded node 'armD'.  
Note: Removed unneeded node 'west\_sreg\_1D'.  
Note: Removed unneeded node 'west\_sreg\_0D'.  
Note: Removed unneeded node 'east\_sreg\_1D'.  
Note: Removed unneeded node 'east\_sreg\_0D'.

f: \warp\bin\topld.exe: No errors.

-----  
PLD Optimizer Software: DSGNOPT.EXE 01/MAR/97 [v4.00] 4 IR x77  
DESIGN HEADER INFORMATION (20:11:22)  
Input File(s): gcr02.pla  
Device : C22V10  
Package : PALCE22V10-5PC  
ReportFile : gcr02.rpt  
Program Controls:  
None.  
Signal Requests:  
None.  
Completed Successfully

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PLD Optimizer Software: DSGNOPT.EXE 01/MAR/97 [v4.00] 4 IR x77  
OPTIMIZATION OPTIONS (20:11:22)  
Messages:  
Information: Process virtual 'east\_next\_sreg\_0' ... expanded.  
Information: Process virtual 'east\_sreg\_0' ... converted to NODE.  
Information: Process virtual 'east\_next\_sreg\_1' ... expanded.  
Information: Process virtual 'east\_sreg\_1' ... converted to NODE.  
Information: Process virtual 'west\_next\_sreg\_0' ... expanded.  
Information: Process virtual 'west\_sreg\_0' ... converted to NODE.  
Information: Process virtual 'west\_next\_sreg\_1' ... expanded.  
Information: Process virtual 'west\_sreg\_1' ... converted to NODE.  
Information: Optimizing logic using best output polarity for signals:  
east\_sreg\_0.D east\_sreg\_1.D west\_sreg\_0.D west\_sreg\_1.D bellout  
  
Information: Selected logic optimization OFF for signals:  
east\_sreg\_0.C east\_sreg\_1.C west\_sreg\_0.C west\_sreg\_1.C arm.D arm.C

Summary:  
Error Count = 0 Warning Count = 0

Completed Successfully  
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PLD Optimizer Software: MNOPT.EXE 19/JUL/96 [v3.22A] 4 IR x77  
LOGIC MINIMIZATION ()  
Messages:  
Summary:

Error Count = 0 Warning Count = 0

Completed Successfully

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PLD Optimizer Software: DSGNOPT.EXE 01/MAR/97 [v4.00] 4 IR x77

OPTIMIZATION OPTIONS (20:11:24)

Messages:

Information: Optimizing Banked Preset/Reset requirements.

Summary:

Error Count = 0 Warning Count = 0

Completed Successfully

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PLD Compiler Software: PLA2JED.EXE 01/MAR/97 [v4.00] 4 IR x77

DESIGN EQUATIONS (20:11:25)

arm D = bellout  
arm AR = GND  
arm SP = GND  
arm C = clk

west\_sreg\_1.D = /west\_sreg\_1.Q \* /gcr1 \* /west\_sreg\_0.Q  
+ west\_sreg\_1.Q \* /gcr1 \* west\_sreg\_0.Q  
+ /blk1 \* west\_sreg\_0.Q  
+ west\_sreg\_1.Q \* /blk1

west\_sreg\_1.AR = GND  
west\_sreg\_1.SP = GND  
west\_sreg\_1.C = clk

west\_sreg\_0.D = /west\_sreg\_1.Q \* /gcr1 \* /west\_sreg\_0.Q  
+ west\_sreg\_1.Q \* blk1 \* /west\_sreg\_0.Q  
+ blk1 \* /gcr1

west\_sreg\_0.AR = GND  
west\_sreg\_0.SP = GND  
west\_sreg\_0.C = clk

east\_sreg\_1.D = /east\_sreg\_1.Q \* /gcr2 \* /east\_sreg\_0.Q  
+ east\_sreg\_1.Q \* /gcr2 \* east\_sreg\_0.Q  
+ /blk2 \* east\_sreg\_0.Q  
+ east\_sreg\_1.Q \* /blk2

east\_sreg\_1.AR = GND  
east\_sreg\_1.SP = GND  
east\_sreg\_1.C = clk

east\_sreg\_0.D = /east\_sreg\_1.Q \* /gcr2 \* /east\_sreg\_0.Q  
+ east\_sreg\_1.Q \* blk2 \* /east\_sreg\_0.Q  
+ blk2 \* /gcr2

east\_sreg\_0.AR = GND  
east\_sreg\_0.SP = GND  
east\_sreg\_0.C = clk

/bellout = west\_sreg\_1.Q \* east\_sreg\_1.Q

Completed Successfully

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PLD Compiler Software: PLA2JED.EXE 01/MAR/97 [v4.00] 4 IR x77

DESIGN RULE CHECK (20:11:25)

Messages: None.  
 Summary: Error Count = 0 Warning Count = 0

Completed Successfully

-----  
 PLD Compiler Software: PLA2JED.EXE 01/MAR/97 [v4.00] 4 IR x77  
 DESIGN SIGNAL PLACEMENT (20:11:25)

Messages:  
 Information: Checking for duplicate NODE logic. None.

C22V10

clk =	1	24	* not used
gcr2 =	2	23	= (west_sreg_1)
blk2 =	3	22	= (west_sreg_0)
gcr1 =	4	21	= bellout
blk1 =	5	20	* not used
not used *	6	19	* not used
not used *	7	18	* not used
not used *	8	17	* not used
not used *	9	16	= arm
not used *	10	15	= (east_sreg_0)
not used *	11	14	= (east_sreg_1)
not used *	12	13	* not used

Summary: Error Count = 0 Warning Count = 0

Completed Successfully

-----  
 PLD Compiler Software: PLA2JED.EXE 01/MAR/97 [v4.00] 4 IR x77  
 RESOURCE ALLOCATION (20:11:25)

Information: Macrocell Utilization.

Description	Used	Max
Dedicated Inputs	4	11
Clock/Inputs	1	1
I/O Macrocells	6	10
11 / 22 = 50 %		

Information: Output Logic Product Term Utilization.

Node#	Output Signal Name	Used	Max
14	east_sreg_1	4	8
15	east_sreg_0	3	10
16	arm	1	12
17	Unused	0	14
18	Unused	0	16
19	Unused	0	16
20	Unused	0	14
21	bellout	1	12
22	west_sreg_0	3	10
23	west_sreg_1	4	8
25	Unused	0	1
16 / 121 = 13 %			

Completed Successfully

-----  
PLD Compiler Software:            PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77

JEDEC ASSEMBLE                    (20:11:25)

Messages:

Information: Output file 'gcr02.jed' created.

Summary:

                  Error Count = 0            Warning Count = 0

Completed Successfully at 20:11:25