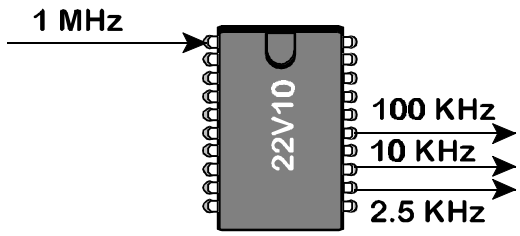
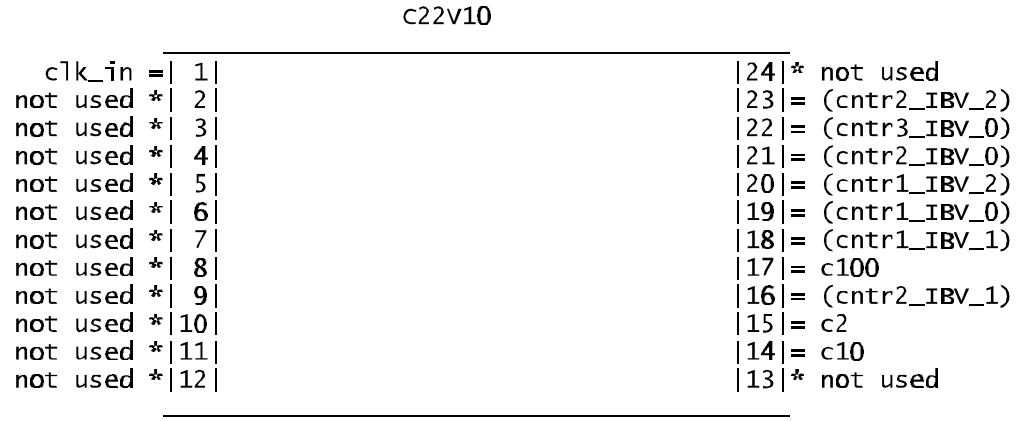
A LABORATORY CLOCK GENERATOR

In some experiments, the 1MHz clock provided may be too fast. Using one 22V10 PAL and a minimal knowledge of VHDL, one can fabricated a clock generator as shown below.

The 22V10 may be programmed with two divide by 10 counters (Decade Counters) and a divide by 4 counter. With a 1MHZ input, this will produce a 100KHZ, a 10KHz and a 2.5 KHz clock source.



The actual pinout that might be obtained is shown below.



The entity description is given below (it is so simple, there is no need to make you figure it out!)

```
entity clock_gen is port(
            clk_in:      in  std_logic;
            c100,c10,c2: out std_logic);
       end clock_gen;
```

You will need, in the architecture part, three integer signals:

```
    signal cntr1,cntr2:integer (0 to 15);
    signal cntr3:integer (0 to 3);
```

From here, with a few if..then..else statements, you should be able to devise this clock generator. It will be a lot easier to use than wiring up several SN74163's to do the job!