WARP2 AND VHDL
A QUICK SNAPSHOT

The VHDL file you write:

```
ENTITY simple IS PORT (a: IN BIT;not_a: OUT BIT);
   END simple;
ARCHITECTURE dataflow OF simple IS
   BEGIN
      not_a<=NOT a;
   END dataflow;
```

The REPORT file you get:

```
     | | | | | | |
   _________________
  -|                 |-
  -|                 |-
  -|                 |-
  -|    CYPRESS      |-
  -|                 |-
  -|                 |-   Warp VHDL Synthesis Compiler: Version 4 IR x77
  -|                 |-   Copyright (C) 1991, 1992, 1993,
   |_________________|    1994, 1995, 1996, 1997 Cypress Semiconductor
     | | | | | | |
========================================================================
Compiling:  invert.vhd
Options:    -q -yv2 -yu -e10 -w100 -o2 -ygs -fK -fF -fN -v10 -dc22v10 -pPALCE22V10-5PC
invert.vhd
========================================================================

f:\warp\bin\vhdlfe.exe V4 IR x77:  VHDL parser
Fri Jan 02 11:15:25 1998
Library 'work' => directory 'lc22v10'
Linking 'f:\warp\lib\common\work\cypress.vif'.
f:\warp\bin\vhdlfe.exe:  No errors.
f:\warp\bin\tovif.exe V4 IR x77:  High-level synthesis
Fri Jan 02 11:15:26 1998
Linking 'f:\warp\lib\common\work\cypress.vif'.
Note:  Removing wires from arch. 'dataflow' of entity 'simple'.
f:\warp\bin\tovif.exe:  No errors.
f:\warp\bin\topld.exe V4 IR x77:  Synthesis and optimization
Fri Jan 02 11:15:28 1998
Linking 'f:\warp\lib\common\work\cypress.vif'.
```

```
Detecting unused logic.
Alias Detection
      Aliased 0 equations, 0 wires.
Circuit simplification
      Substituting virtuals - pass 1:

Circuit simplification results:
       Expanded 0 signals.
       Turned 0 signals into soft nodes.
       Maximum expansion cost was set at 10.
Created 2 PLD nodes.
f:\warp\bin\topld.exe:  No errors.
```

```
PLD Optimizer Software:       DSGNOPT.EXE    01/MAR/97    [v4.00 ] 4 IR x77
DESIGN HEADER INFORMATION  (11:15:31)
Input File(s): invert.pla
Device        : C22V10
Package       : PALCE22V10-5PC
ReportFile    : invert.rpt
Program Controls:  None.
Signal Requests:
    GROUP KEEPPOL ALL
    GROUP FLOAT ALL

Completed Successfully
```

```
PLD Optimizer Software:       DSGNOPT.EXE    01/MAR/97    [v4.00 ] 4 IR x77
OPTIMIZATION OPTIONS       (11:15:31)
Messages:   Information: Selected logic optimization OFF for signals: not_a
Summary:    Error Count = 0      Warning Count = 0
Completed Successfully
```

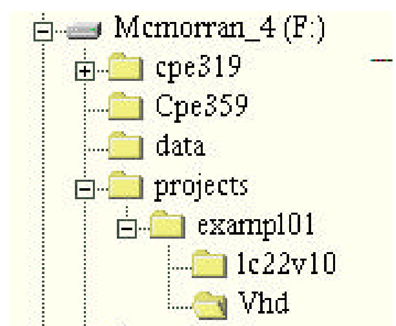
```
PLD Optimizer Software:       MINOPT.EXE     19/JUL/96    [v3.22A] 4 IR x77
LOGIC MINIMIZATION          ()
Messages:
Summary:        Error Count = 0      Warning Count = 0
Completed Successfully
------------------------------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    01/MAR/97    [v4.00 ] 4 IR x77
OPTIMIZATION OPTIONS        (11:15:32)
Messages:   Information: Optimizing Banked Preset/Reset requirements.
Summary:   Error Count = 0      Warning Count = 0
Completed Successfully
------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77
DESIGN EQUATIONS            (11:15:33)
   not_a =  /a
Completed Successfully
------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77
DESIGN RULE CHECK           (11:15:33)
Messages:          None.
Summary:          Error Count = 0      Warning Count = 0
Completed Successfully
```

```
PLD Compiler Software:        PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77
DESIGN SIGNAL PLACEMENT     (11:15:33)
Messages:   Information: Checking for duplicate NODE logic.      None.

                                C22V10
                  __________________________________________
             a =| 1|                                  |24|* not used
       not used *| 2|                                  |23|* not used
       not used *| 3|                                  |22|* not used
       not used *| 4|                                  |21|* not used
       not used *| 5|                                  |20|* not used
       not used *| 6|                                  |19|* not used
       not used *| 7|                                  |18|* not used
       not used *| 8|                                  |17|* not used
       not used *| 9|                                  |16|* not used
       not used *|10|                                  |15|* not used
       not used *|11|                                  |14|= not_a
       not used *|12|                                  |13|* not used
                  __________________________________________
Summary:             Error Count = 0      Warning Count = 0
Completed Successfully
```

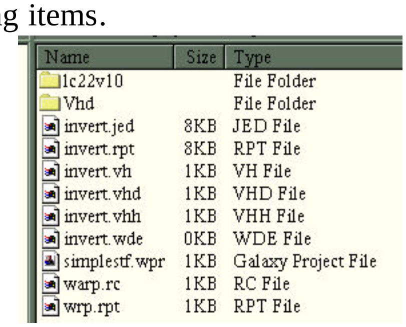
```
PLD Compiler Software:         PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77
RESOURCE ALLOCATION         (11:15:33)
 Information: Macrocell Utilization.
                    Description        Used      Max
                ______________________________________
                | Dedicated Inputs   |     0  |    11   |
                | Clock/Inputs       |     1  |     1   |
                | I/O Macrocells     |     1  |    10   |
                ______________________________________
                                           2   /    22    = 9    %
  Information: Output Logic Product Term Utilization.
                 Node#  Output Signal Name  Used    Max
                ________________________________________
                | 14   |  not_a              |   1  |    8   |
                | 15   |  Unused             |   0  |   10   |
                | 16   |  Unused             |   0  |   12   |
                | 17   |  Unused             |   0  |   14   |
                | 18   |  Unused             |   0  |   16   |
                | 19   |  Unused             |   0  |   16   |
                | 20   |  Unused             |   0  |   14   |
                | 21   |  Unused             |   0  |   12   |
                | 22   |  Unused             |   0  |   10   |
                | 23   |  Unused             |   0  |    8   |
                | 25   |  Unused             |   0  |    1   |
                ________________________________________
                                              1   / 121    = 0    %

Completed Successfully
------------------------------------------------------------------------------
PLD Compiler Software:         PLA2JED.EXE    01/MAR/97    [v4.00 ] 4 IR x77
JEDEC ASSEMBLE              (11:15:33)
Messages:   Information: Output file 'invert.jed' created.
Summary:    Error Count = 0      Warning Count = 0
Completed Successfully at 11:15:33
```

If you were to read this report carefully, you would find that six different software programs ("tools") were used in this process. We will discuss them later. Finally, the JEDEC Fuse file is produced. We will not look at this file now, it is not generally for human consumption anyway.

A little bit of information on using WARP2 and its installation. Each **PROJECT** you work on should be placed in a separate directory. An example of this is shown to the right. For this example, a root directory called "projects" was created. This particular design was placed in a subdirectory called "exampl01." To begin with, all that was placed in this subdirectory was the "invert.vhd" source file and a "simpstff.wpd" Warp Project Description file.



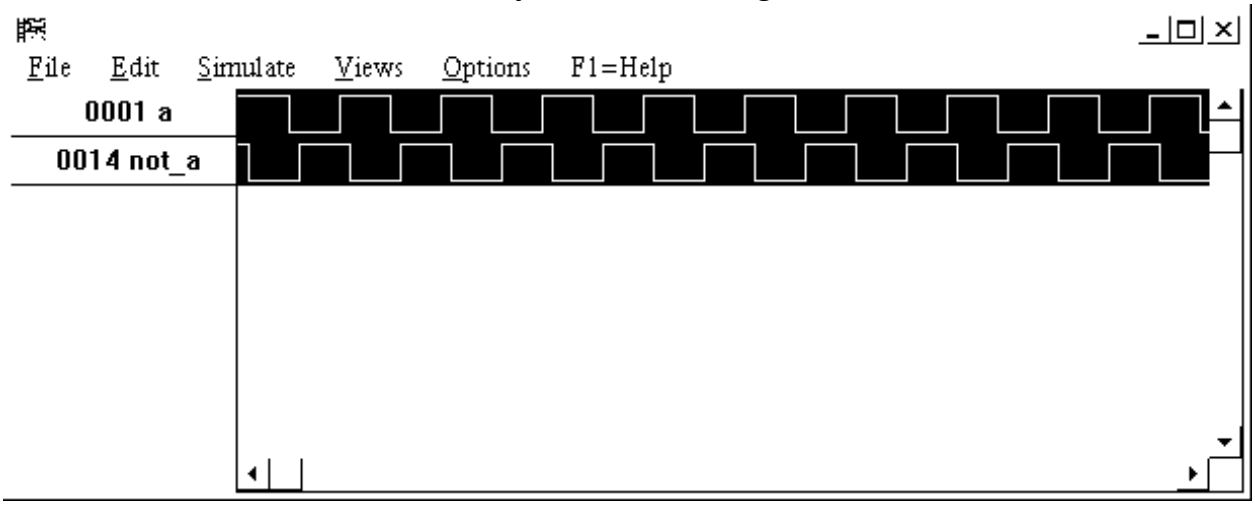
Once the file is compiled, this subdirectory contains the following items. Nine files, six of which are named "invert" and are the VHDL file, the REPORT file, the JEDEC file, and three intermediate files. There is the WPD file and two WARP files. In addition, two subdirectories were created with files in them too. If you do not put each project in a separate subdirectory, you will have one terrible time trying to delete a single project from your disk!



Name	Size	Type
lc22v10		File Folder
Vhd		File Folder
invert.jed	8KB	JED File
invert.rpt	8KB	RPT File
invert.vh	1KB	VH File
invert.vhd	1KB	VHD File
invert.vhh	1KB	VHH File
invert.wde	0KB	WDE File
simplestf.wpr	1KB	Galaxy Project File
warp.rc	1KB	RC File
wrp.rpt	1KB	RPT File

Once the JEDEC file has been created, it may be used to program your PLD. It may also be

used with the NOVA simulator to verify that what is being loaded into the PLD works.



You will note that not_a is the inverse a but delayed. Apparently, the design works!