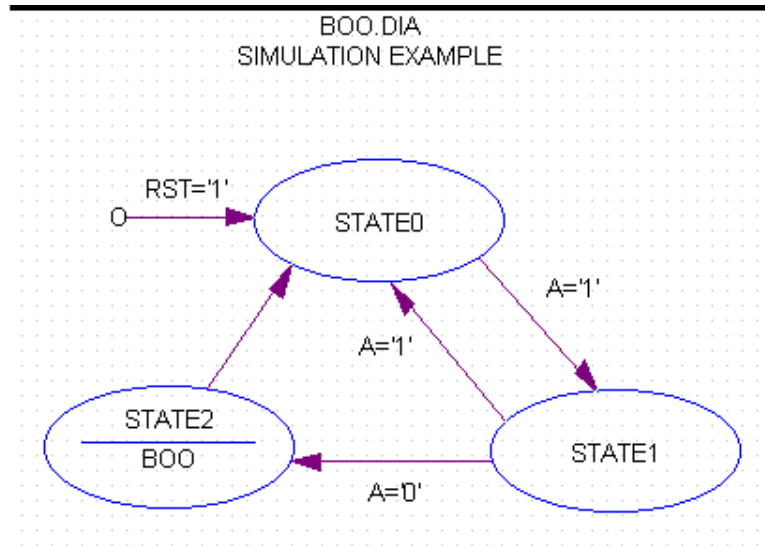


SIMULATION IN STATECAD

Designing with StateCAD allows you to test the design through simulation. This is a brief description of the process. We shall use the following as an example.



While still in StateCAD, under options, select SIMULATE. This brings up the simulation window.

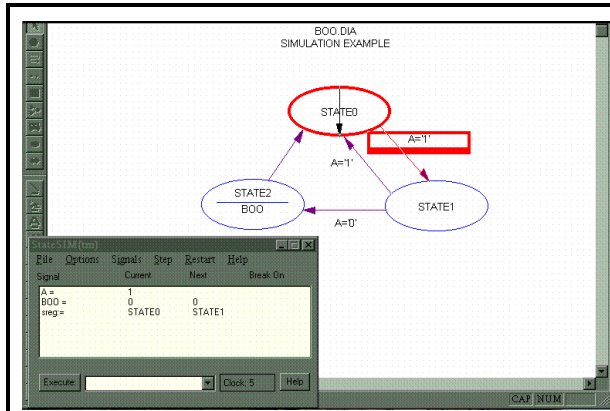
BOO.DIA
SIMULATION EXAMPLE

Signal	Current	Next	Break On
A =	0		
BOO =	0	0	
sreg =	STATE0	STATE0	

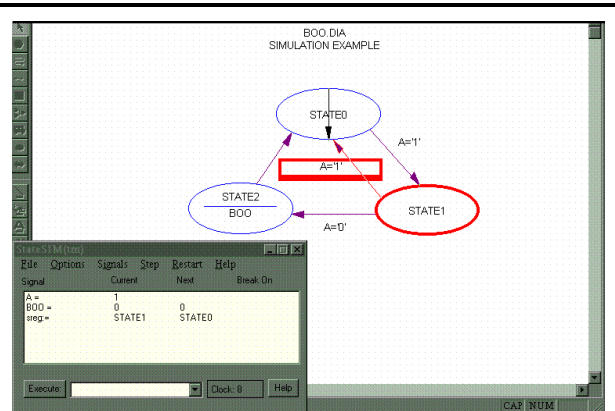
Execute: Clock: 0 Help

CAP NUM

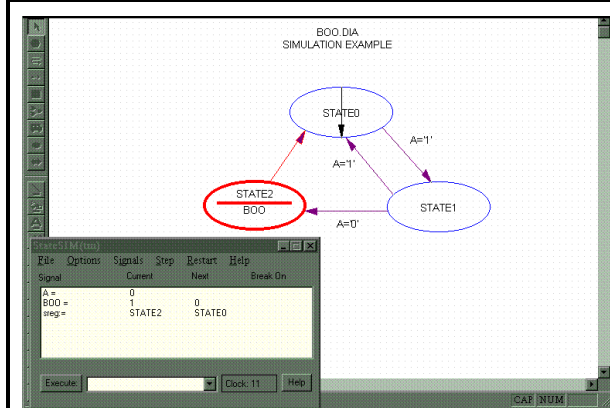
Simulation must be done manually at first. The manual simulation may be saved in a file and rerun. This is accomplished by selecting FILES/RECORD CMD FILE. The you would start the process by selecting SIGNALS/ASSIGN VALUE to set the initial state. Then by using SIGNALS/SELECT VALUE and STEP, you can step the machine through the states, recording the commands and results as you go. This is demonstrated below.



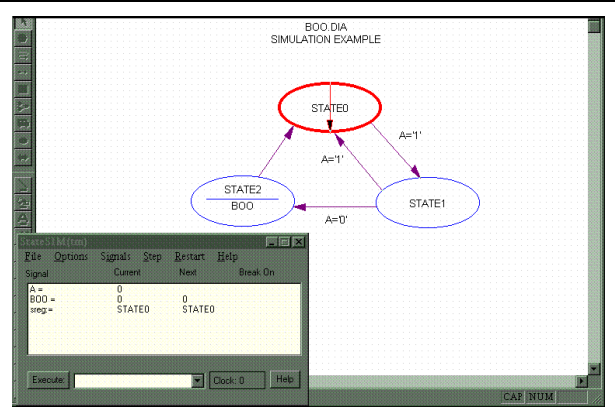
In State 0, ready to go to State 1



At State 1, ready to return to State 0



Reaches State 2. ready to return to State 0



Returned to State 0

The command file generated by this is shown below.

```
log B00.log
restart
radix decimal
errcnt on
cover on
h RST
-----
Clock=0
cycle
check B00 0
-----
Clock=1
cycle
check B00 0
-----
Clock=2
cycle
```

```
check B00 0
l RST
-----
Clock=3
cycle
check B00 0
-----
Clock=4
cycle
check B00 0
-----
Clock=5
cycle
check B00 0
h A
-----
Clock=6
```

```
cycle
check B00 0
-----
Clock=7
cycle
check B00 0
-----
Clock=8
cycle
check B00 0
-----
Clock=9
cycle
check B00 0
-----
Clock=10
cycle
```

```

check B00 0
l A
|-----
| Clock=11
cycle
check B00 1
|-----
| Clock=12
cycle
check B00 0
|-----
| Clock=13
cycle
check B00 0
|-----
| Clock=14
cycle
check B00 0
errcnt show
| No errors found

```

during simulation
errcnt off
cover show
| All 6 transitions
have been followed
cover off
log

The lines with |----- are comment lines. The other lines are as listed below.

```

restart
radix decimal
errcnt on
cover on
h RST

```

These say to (1) restart the simulation, display results in decimal, check errors encountered, check coverage, and set the RST signal (not shown in the diagram) to 1 (high).

```

cycle
check B00 0

```

These say to clock (cycle) the machine and check output BOO, which it found was 0.

```

l RST

```

This says to set RST to 0 (low).

```

h A

```

This says set A to 1 (high). Finally, at the end,

```

errcnt show
| No errors found during simulation
errcnt off
cover show
| All 6 transitions have been followed
cover off
log

```

It shows that no errors were encountered during the simulation and that all 6 possible transitions were tested. The animation feature may be turned on, the Single step turned off, and the command FILES/RUN CMD FILE used to redo the simulation in animated form (i.e. it moves through the states without you having to do anything).

The best way to learn how this simulation works is to use it and try it out.