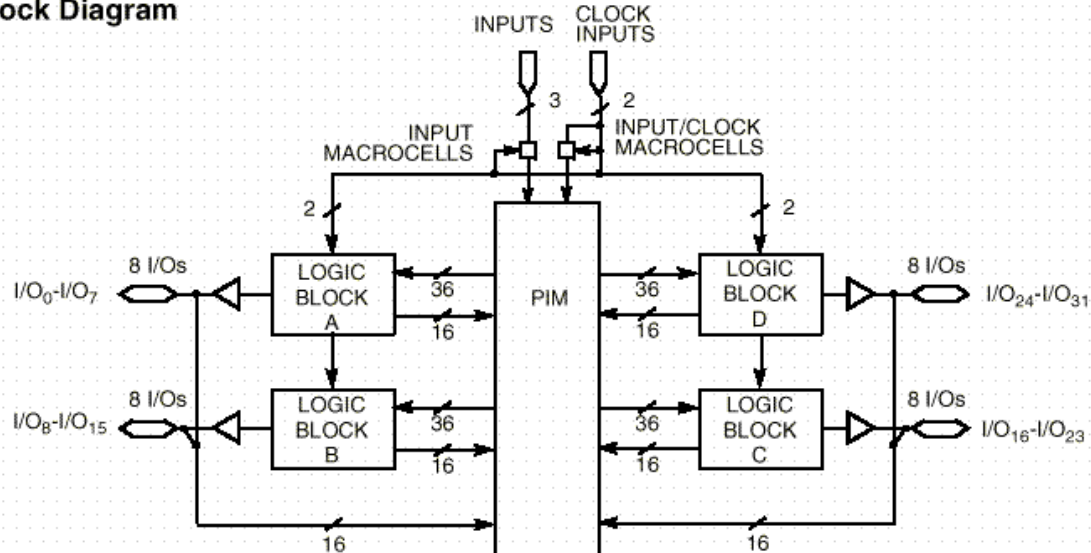


# INTERPRETING WARP2'S REPORT FILE

## WHAT DOES IT ALL MEAN?

A full report file from wARP2 contains a lot of information. Some of it is not of particular importance to you, some is. We shall look at the more important features. First, the **Macrocell utilization data**. This tells you how much of the device is being used by your design. To understand the information provided, consider the 372i CPLD.

### Logic Block Diagram



It consists of 2 identical blocks. Each block has a 72 x 86 Fuse matrix (36 inputs and their complements, 80 general product terms + 2 clock terms + 4 output enable terms). There are a total of 32 macrocells in each block (16 output cells and 16 buried cells). The two blocks are connected, along with 2 clock/input cells and 3 dedicated input cells, to a Programmable Interconnect matrix. This PIM has a total of 156 inputs and 144 outputs.

### Information: Macrocell Utilization.

Description	Used	Max
Dedicated Inputs	3	3
Clock/Inputs	2	2
I/O Macrocells	25	32
Buried Macrocells	8	32
PIM Input Connects	49	156

$$87 / 225 = 38 \%$$

This information is shown in the table above, along with the usage for a particular design. In this example, 38% of the device is used, a somewhat meaningless statistics since it is based on summing up all of the facilities. More detailed information follows this table.

	Required	Max (Available)
CLOCK/LATCH ENABLE signals	0	2
Input REG/LATCH signals	0	37
Input PIN signals	5	5
Input PINs using I/O cells	9	9
Output PIN signals	16	23
Total PIN signals	30	37
Macrocells Used	24	64
Unique Product Terms	84	320

First, we see that neither of the clock inputs was used **as a clock input**. Likewise, none of the inputs needed synchronization (usually provided by the dedicated input pins but also provided by the output cells). It does show, however, that the 2 clock and 3 dedicated input pins (2+3=5) were used as inputs or, in this case, 4 inputs and one node. Nine of the inputs used “output macrocell” pins. The remaining 4 inputs (not listed) used pins on macrocells being used as buried macrocells. Nine of the I/O pins/macrocells were used as outputs. Seven of the I/O macrocells were used as buried macrocells. Eight of the buried macrocells were used.

Thus 24 Macrocells were actually used out of the 64 available. with nine pins of additional macrocells used as inputs, a total of 33 macrocells are accounted for, leaving 31 free.

The question is, “What percentage of the device has been used?” 24/64 or 37.5% of the macrocells were used. 84/320 or 26.25% of the Product terms were used. 49/156 or 31.4% of the PIM inputs were used. The point is, if 100% of the macrocells are used, it makes no difference what the percentage of PIM inputs or P.Terms are used. The same reasoning follows for the other two. All one can really say is that if the percentage of any of these, especially the Product Terms, is way out of line with the others, you probably need to reformulate your design.

If you want additional details, this section of the REPORT file is preceded by details for each of the blocks.

## **THE PINOUT**

A very critical part of the report files in the pin out.

Device: c372i

Package: CY7C372I-125JC

1 : GND	17 : s_7	32 : b_0
2 : a_1	18 : s_1	33 : a_0
3 : b_3	19 : s_6	34 : GND
4 : a_4	20 : s_4	35 : b_1
5 : b_6	21 : s_2	36 : co
6 : a_7	22 : VCC	37 : (p_4) a_2
7 : Not Used	23 : GND	38 : (c_1) b_4
8 : Not Used	24 : b_2	39 : (c_5) a_5
9 : Not Used	25 : a_3	40 : (c_4) b_7
10 : ci	26 : b_5	41 : (p_0)
11 : VPP	27 : a_6	42 : (p_3)
12 : GND	28 : Not Used	43 : (p_7)
13 : c_0	29 : Not Used	44 : VCC
14 : s_0	30 : Not Used	
15 : s_3	31 : Not Used	
16 : s_5		

It is not necessary to comment on the importance of this.

Another important piece of information is found in the section labeled:

### Worst Case Path Summary

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$$t_{PD} = 22.0 \text{ ns for } s_3$$

As the title indicates, this gives the limiting factor for the speed of the device. This section is preceded by timing specifications for each of the outputs.

If the device utilization seems poor for the design you are doing, you will probably want to examine the following section.

### DESIGN EQUATIONS

(14: 56: 06)

$$\begin{aligned} s_7 &= \\ &+ a_7 * /b_7 * /c_7. \text{CMB} \\ &+ /a_7 * b_7 * /c_7. \text{CMB} \\ &+ /a_7 * /b_7 * c_7. \text{CMB} \\ &+ a_7 * b_7 * c_7. \text{CMB} \\ \\ s_6 &= \\ &+ a_6 * /b_6 * /c_6. \text{CMB} \\ &+ /a_6 * b_6 * /c_6. \text{CMB} \\ &+ /a_6 * /b_6 * c_6. \text{CMB} \\ &+ a_6 * b_6 * c_6. \text{CMB} \\ \\ s_5 &= \\ &+ a_5 * /b_5 * /c_5. \text{CMB} \\ &+ /a_5 * b_5 * /c_5. \text{CMB} \\ &+ /a_5 * /b_5 * c_5. \text{CMB} \\ &+ a_5 * b_5 * c_5. \text{CMB} \quad \text{etc.} \end{aligned}$$