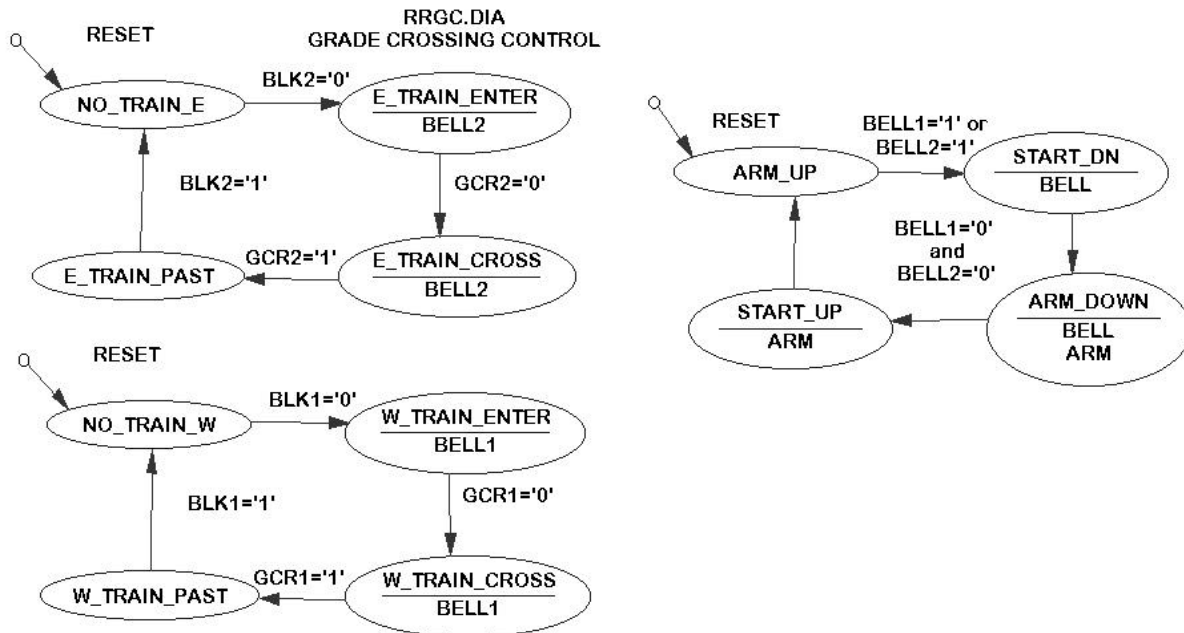


## ANOTHER GRADE CROSSING IMPLEMENTATION DESIGNING THE CONTROLLER ENTIRELY IN STATECAD

The controller may be created completely in StateCAD (using the same general design philosophy) as shown in the StateCAD diagram below.



The upper left-hand corner has the EAST train controller. Below that is the WEST train controller. An interesting ability in StateCAD is that, having draw the EAST controller, all that was necessary to do the WEST controller is (a) SELECT/ALL, COPY, and then PASTE, moving the WEST controller below the EAST one. In doing this, StateCAD changed the state names and left everything else the same. All that was left to do was enter new state names and modify the names of the input and output signals.

The controller on the right hand side combines the outputs of the other two. It only had to have three states, but by adding the `START_UP` state, the number of macrocells could be reduced. This is because, by doing this, `BELL` becomes one of the state variables and `ARM` the other. The report file shows the following:

### RESOURCE ALLOCATION (15:22:12)

#### Information: Macrocell Utilization.

Description	Used	Max
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<b>Dedicated Inputs</b>	<b>5</b>	<b>11</b>
<b>Clock/Inputs</b>	<b>1</b>	<b>1</b>
<b>I/O Macrocells</b>	<b>6</b>	<b>10</b>

$$12 / 22 = 54 \%$$

**Information: Output Logic Product Term Utilization.**

<b>Node#</b>	<b>Output Signal Name</b>	<b>Used</b>	<b>Max</b>
14	bell	5	8
15	sreg_0	3	10
16	sreg1_0	3	12
17	Unused	0	14
18	Unused	0	16
19	Unused	0	16
20	Unused	0	14
21	arm	1	12
22	sreg1_1	3	10
23	sreg_1	3	8
25	Unused	0	1

$$18 / 121 = 14 \%$$

Only six macrocells were required. But we know three state machines, each with four states, will require six macrocells. Hence the outputs require no additional cells. Note, also, above, that only sreg (the EAST machine) and sreg1 (the WEST machine) show up on the list of macrocells used. Again, "Bell" and "ARM" are the state variables for the third machine.