



COMPUTER ENGINEERING PROGRAM



California Polytechnic State University

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CPE 269 Experiment 1



Constrained Up/Down Counter

Objectives:

- To review the Xilinx Design Methodology
- To review VHDL behavioral modeling of FSMs
- To review VHDL structural modeling
- To design a design a digital system that meets various design constraints

Somewhat Meaningful Comments: This experiment is primarily a review from of digital circuits that you have modeled in previous digital design courses. The slight twist in this experiment is that you need to assemble your various VHDL models into a system under a few simple constraints provided by the problem description.

Assignment: Design a three-bit up/down counter that adheres to the following constraints:

- The counter uses a normal sequence (0, 1, 2, 3, ...7)
- The counter-driver is specified using VHDL behavioral modeling
- The counter-driver has one internal input: the slow clock from the clock divider module. The clock divider circuit is provided for you so you don't need to design it.
- The output of the counter is displayed in decimal on one 7-segment display
- The entire system uses VHDL structural modeling of at least two levels
- The box labeled "other circuitry" in Figure 1 has two inputs: UP_DOWN and the output of the counter driver. The SEGMENTS and DISP_EN are used to drive on 7-segment display on the Nexys board (non-used displays should be turned off).
- The UP_DOWN input should be attached to BTN0 on the Nexys board.

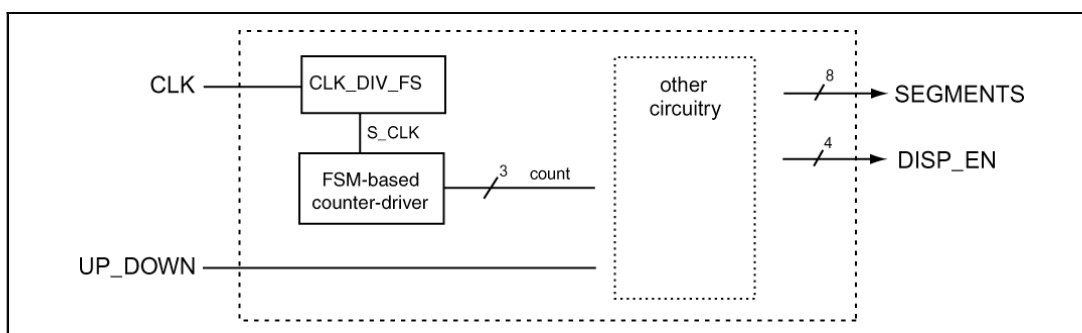


Figure 1: Partial block diagram for the up/down counter.

Deliverables:

1. Demonstrate a working design to the lab instructor or Teaching Assistant.
2. A standard lab report. See description of lab report for details.

Questions:

1. Briefly describe what the term “methodology” means in the phrase “Xilinx Design Methodology”.
 2. Would it have been possible to implement this counter with a flat design? In other words, did you really need to use structural modeling? Briefly explain. The advantages of using a multi-level design for this counter.
 3. Would it have been possible to implement this entire design using only a VHDL FSM behavioral model? Briefly explain your approach on this matter.
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