



COMPUTER ENGINEERING PROGRAM

California Polytechnic State University

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CPE 269 Experiment 3



FSM-Based Sequence Detectors using VHDL Behavioral Modeling

Objectives:

- To design and implement a FSM that can be used for something relatively useful.
- To experience the pure joy of designing and testing a non-trivial FSM

Somewhat Meaningful Comments: The design of sequence detectors using FSMs is one of the more basic uses for a FSM. The designs are not overly complicated yet provided immediate gratification to the FSM designers. After you attempt a few sequence detector designs, you more than likely agree that they are not overly complicated. For this lab activity, we'll add a few inputs to make the design something more than the typical one control input FSM.

Assignment: Design a sequence detector that will detect the sequences as described below. Drop your FSM designs into the circuit shown in Figure 1. The SEQ_DVR block is used to sequentially provide the switch inputs to the FSM. In other words, the switches are used to form the "test" sequence. The BC_DEC is used to display a happy message once the correct sequence is detected on the switches.

- Use a Moore-type FSM that does not reset once the sequence is found.
- The SQ2 and SQ5 inputs determine which sequence is detected according to Table 1. Connect SQ2 and SQ5 to BTN3 and BTN2 on the development board. Consider SQ2 and SQ5 to be positive logic inputs.
- Minimize your use of states in the FSM; use no more than ten states for this FSM.

SQ2	SQ5	Sequence
0	0	"010000"
0	1	"010010"
1	0	"011000"
1	1	"011010"

Table 1: The sequences of choice.

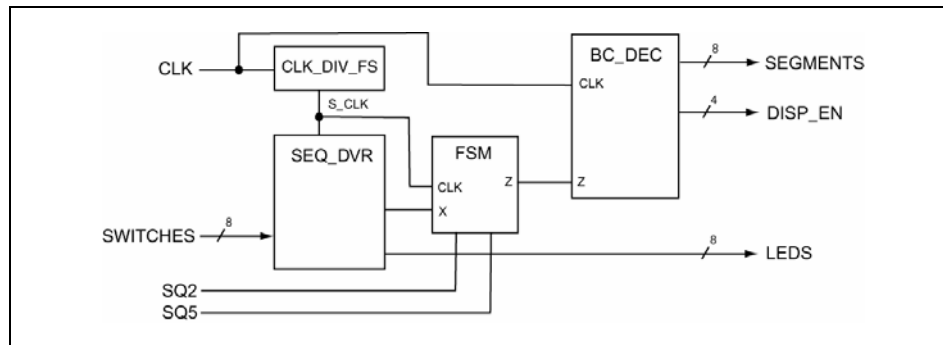


Figure 1: The top-level circuit for testing the sequence detector.

Deliverables:

1. Demonstrate your working circuit to the lab instructor or Teaching Assistant.
2. Answers to the questions below.

Questions:

1. Briefly describe an application where sequence detectors could potentially be useful.
2. Where in this circuit could you consider a parallel to serial conversion occurring? Briefly explain.
3. Provide a Mealy-type state diagram for these FSM designed in this lab activity under the conditions that the FSM resets once the desired sequence is detected.