



COMPUTER ENGINEERING PROGRAM



California Polytechnic State University

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CPE 269 Experiment 4



FSM Application in a Control Unit/Datapath System Model

Objectives:

- To use a FSM as a Control Unit to control a given Datapath
- To understand and apply a VHDL behavioral description of a universal shift register

Somewhat Meaningful Comments: The most common application of FSMs is to act as a controller. In other words, FSMs are circuit used to control other circuits. For this lab activity, we'll be designing the FSM to work with a Universal Shift Register using the *control unit* and *datapath model*. In this model, shown in Figure 1, the FSM is the control unit while the datapath is the circuit being controlled. The Control Unit and the Datapath communicate through the *control* and *status* signals.

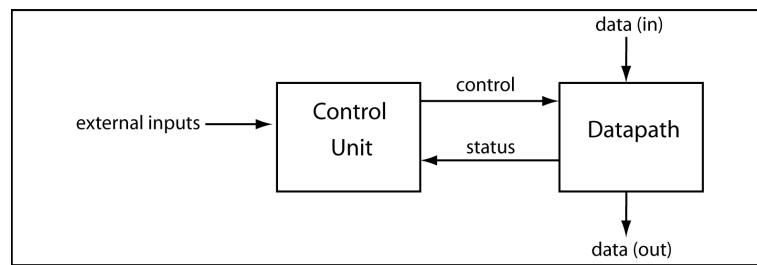


Figure 1: The

Control Unit-Datapath model.

A Universal Shift Register (USR) is a common digital circuit. The term “universal” refers to the fact that it can do a few more functions than a simple shift. The model of the shift register that is used in this experiment is shown in Figure 2 along with a brief description of the device I/O. The VHDL code for this circuit is provided on the class website. Figure 3 and Figure 4 indicate how inputs DR_IN and DL_IN affect the shift-left and shift-right operations, respectively.

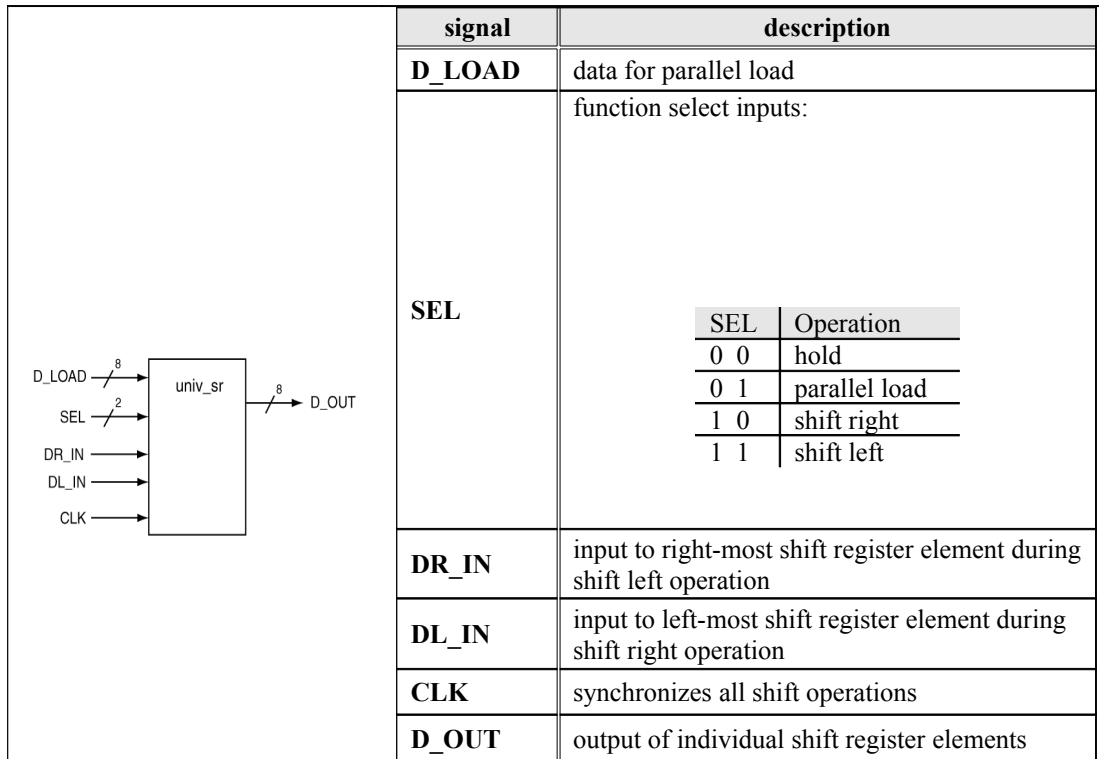


Figure 2: Universal shift register model and description.

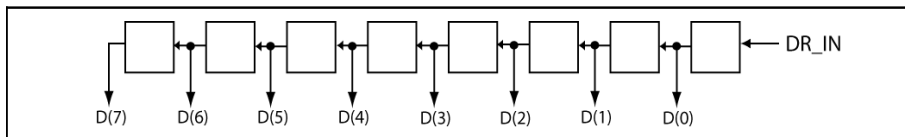


Figure 3: How

inputs DR_IN input affects the shift-left operations.

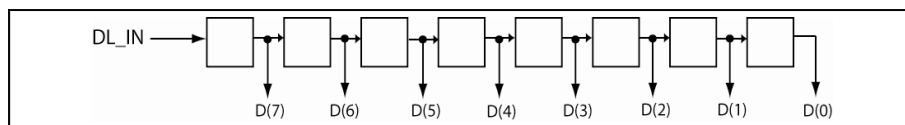


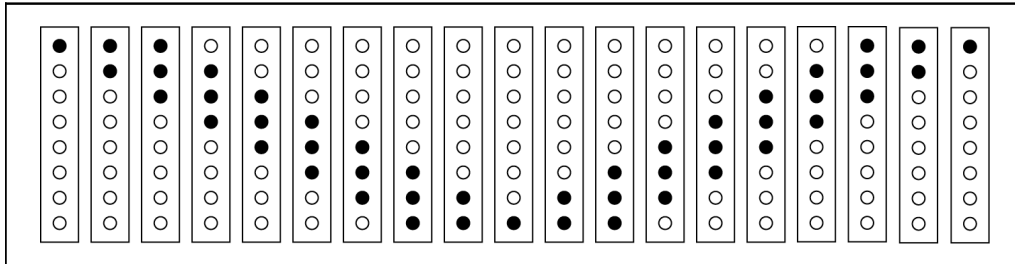
Figure 4: How

inputs DL_IN input affects the shift-right operations.

Assignment: Implement a circuit that will continuously display the output shown in Figure 5. This figure can be considered a rough representation of an eight LED display similar to the LEDs on the development board. The displays are shown sideways to save space; the MSB position is the left-most LED. The filled in circles represent lit LEDs. Figure 5 shows how the 8-LED display changes with rising edges of the system clock. The final circuit should appear something like what is shown in Figure 6.

- Use a clock divider, FSM, and an USR in your design. The USR is provided (VHDL model) as part of the experiment but you're not allowed to alter the model. The clock divider is also provided for you.
- Use no more than nine states in your final design.
- Minimize the number of control outputs from the FSM.

- The DE input control the functioning of the shifting action. When DE is asserted, the display appears as the left-most display diagram and starts the shifting action shown in Figure 5 on the next clock edge following the assertion of DE. When the DE input is not asserted, the shifting stops at the current display.
- Consider DE to be an active high input.
- The DE input should be connected to BTN3 on the development board.
- The outputs of the USR should drive the LEDs on the development board.



Figure

5: The top-level circuit for testing the sequence detector.

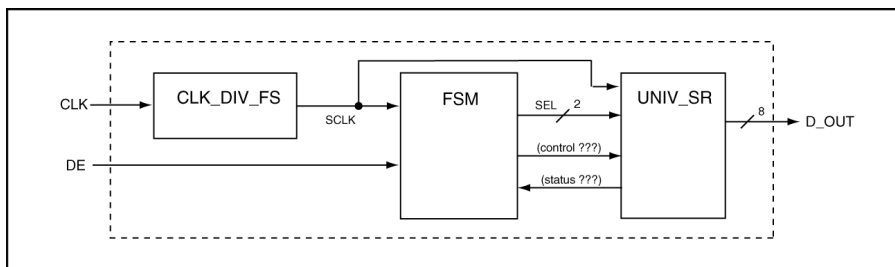


Figure 6: The top-

level circuit diagram.

Deliverables:

1. Demonstrate your working circuit to the lab instructor or Teaching Assistant.
2. Answers to the questions below.

Questions:

1. The number of states in the final FSM were purposely limited in this lab activity. If you implemented a FSM that directly output the desired LED patterns, how many states would there be in the state diagram? Briefly describe at least two reasons for limiting the number of states in a given state diagram.
2. For this experiment, you used either a Mealy or Moore-type FSM. Briefly justify why you choose the FSM type used you used. Discuss the advantages or disadvantages of using one type of FSM over another for a design such as the one you implemented in this experiment.
3. You used an 8-bit universal shift register (USR) in this experiment. Use the VHDL model for this USR to create a 24-bit universal shift register using three 8-bit USRs. Figure 7 shows the final block diagram for this device. Your solution should use structural modeling and instantiate the required number of 8-bit USRs used in this experiment.

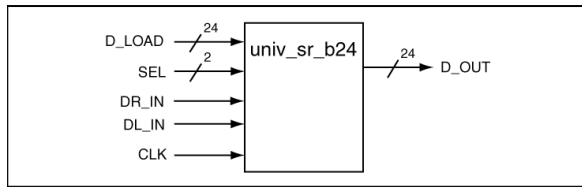


Figure 7: The black box diagram for Question