



# COMPUTER ENGINEERING PROGRAM



California Polytechnic State University  
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## CPE 269 Experiment 5



### Developing a Relatively Simple Datapath

#### Objectives:

- To use RTL equations to specify and generate hardware requirements
- To understand and implement VHDL behavioral descriptions of a typical datapath

**Somewhat Meaningful Comments:** The *datapath* is generally a circuit that contains the hardware required to implement a given set of microoperations. As shown in Figure 1, the datapath is able to implement these operations under control of the *control unit*. The datapath is generally comprised of registers and register-based components but can also contain combinatorial elements.

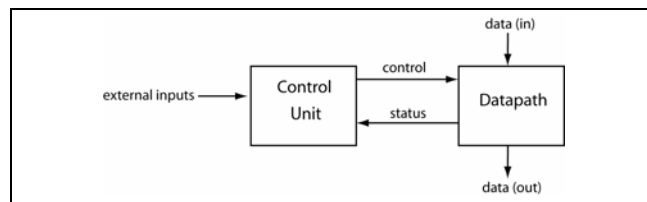


Figure 1: The Control Unit-Datapath model.

**Assignment:** Design a datapath that can implement the RTL equations shown in Table 1. Make sure your design is as hardware efficient as possible. Figure 1 shows the top-level diagram for testing your final circuit. Use the connection matrix in Table 2 to connect your final circuit to the development board. Additionally, your circuit should adhere to the following guidelines:

- All registers should be RET and contain an asynchronous input that clears the register (CLR).
- All registers should have 4-bit width except for ACC which should be 8-bits wide.
- Connect the slow clock to the right-most LED for a continuous sanity check.

Mnemonic	RTL	Comment
LDRA	$LDA, \overline{LDB} : REGA \leftarrow SW74$	Load REGA with the contents of the upper four switches
LDRB	$\overline{LDA}, LDB : REGB \leftarrow SW30$	Load REGB with the contents of the lower four switches
LDRC	$\overline{MX}, LDACC : ACC \leftarrow REGA$ $MX, LDACC : ACC \leftarrow REGB$	Load the ACC with the contents of either REGA or REGB.

Table 1: RTL equations describing requirements of datapath.

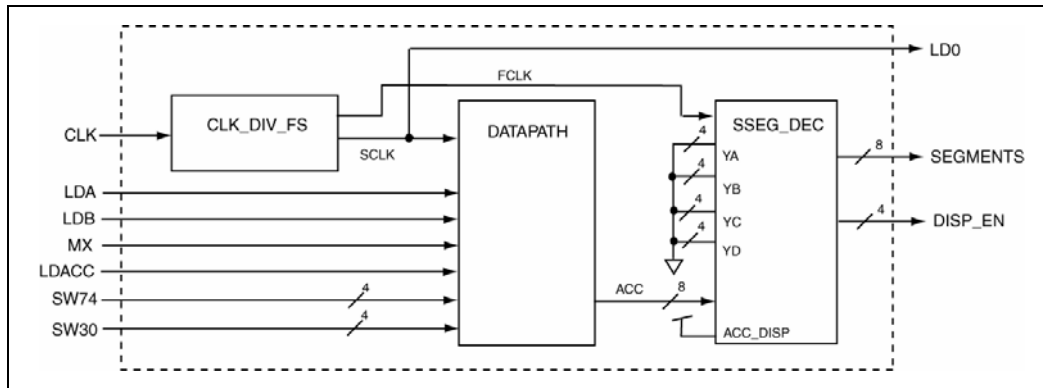


Figure 2: The final circuit diagram.

Development Board Connections			
LDA	LDB	MX	ACC
BTN3	BTN2	BTN1	BTN0

Table 2: Development Board Connection Matrix.

### Deliverables:

1. Demonstrate your working circuit to the lab instructor or Teaching Assistant.
2. Answers to the questions below.

### Questions:

1. Briefly but complete describe the operation of the final circuit in this experiment.
2. What is least number of clock cycles required to display the contents of the left-most switches on the 7-segment display.
3. Briefly speculate on why the CLR input on the registers was required but not used in this experiment.
4. Browse through the SSEG\_DEC VHDL model and briefly describe what the YA, YB, YC, and YD inputs would do if they were in fact used in this experiment.
5. Browse through the SSEG\_DEC VHDL model and determine describe how the ACC\_DISP input affects the 7-segment display.