FINAL EXAM #2

EE347 F96

Print Your Name:_____

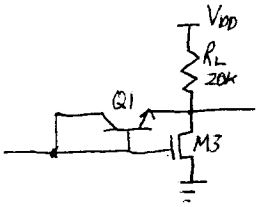
I observed the honor code that holds me responsible for my own work and responsible for my own actions with regard to this test.

Signature: _____

Part 1 (50 Points)	
Part 2 (25 Points)	
Part 3 (25 Points)	
Total (100 Points)	

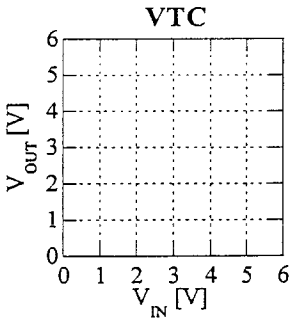
1. Consider the following PSPICE circuit file.

```
* EE 347 Final
Vin  2 0
Vdd  1 0 5.0
RL   1 3 20K
M3   3 2 0 0 NMOD1
Q1   2 2 3 CA3086

.MODEL NMOD1 NMOS (L=3U W=6U KP=69U GAMMA=0.37
+LAMBDA=0.06 RD=1 RS=1 VTO=1.0 TOX=0.04U
+CBD=2F CBS=2F CJ=200U CGBO=200P CGSO=40P CGDO=40P)

.MODEL PMOD1 PMOS (L=3U W=6U KP=34.5U GAMMA=0.37
+LAMBDA=0.06 RD=1 RS=1 VTO=-1.0 TOX=0.04U
+CBD=2F CBS=2F CJ=200U CGBO=200P CGSO=40P CGDO=40P)

.MODEL CA3086 NPN (BF=100 CJE=0.6p CJC=0.58p CJS=2.8p
+VJE=0.7)

.DC Vin 0.0 5.0 0.01
.OP

.PROBE
.END
```



A) Sketch the circuit diagram corresponding to it.

B) Build the circuit and measure the voltage transfer characteristic [VTC]. Please sketch the VTC on the axes provided below and ask your instructor to verify your measurement.



C) What is the value of V_M?

FINAL EXAM #6

EE347 F96

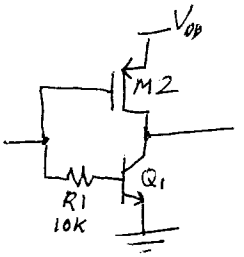
Print Your Name:_____

I observed the honor code that holds me responsible for my own work and responsible for my own actions with regard to this test.

Signature: _____

Part 1 (50 Points)	
Part 2 (25 Points)	
Part 3 (25 Points)	
Total (100 Points)	

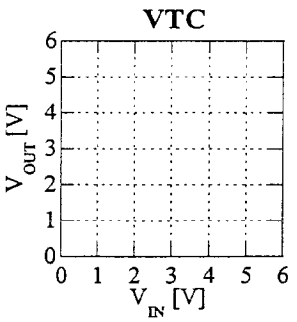
1. Consider the following PSPICE circuit file.




```
* EE 347 Final
Vin  3 0
Vdd  1 0 5.0
R1   3 4 10K
M2   2 3 1 1 PMOD1
Q1   2 4 0   CA3086

.MODEL NMOD1 NMOS (L=3U W=6U KP=69U GAMMA=0.37
+LAMBDA=0.06 RD=1 RS=1 VTO=1.0 TOX=0.04U
+CBD=2F CBS=2F CJ=200U CGBO=200P CGSO=40P CGDO=40P)

.MODEL PMOD1 PMOS (L=3U W=6U KP=34.5U GAMMA=0.37
+LAMBDA=0.06 RD=1 RS=1 VTO=-1.0 TOX=0.04U
+CBD=2F CBS=2F CJ=200U CGBO=200P CGSO=40P CGDO=40P)

.MODEL CA3086 NPN (BF=100 CJE=0.6p CJC=0.58p CJS=2.8p
+VJE=0.7)

.DC Vin 0.0 5.0 0.01
.OP

.PROBE
.END
```

A) Sketch the circuit diagram corresponding to it.

B) Build the circuit and measure the voltage transfer characteristic [VTC]. Please sketch the VTC on the axes provided below and ask your instructor to verify your measurement.



C) What is the value of V_M?

2. In the laboratory experiments this quarter, you have had the opportunity to build and test several different types of digital logic gates from several logic families. Consider the following logic families: CMOS, TTL, and ECL. For each, describe at least one advantage, one disadvantage, and a typical application you might choose to use it in rather than selecting a design based on the other logic families.

CMOS

ADV. VERY LOW POWER
SMALL DEVICES = HIGH DENSITY
RAIL-TO-RAIL LOGIC SWING

DIS-AD GENERALLY SLOWER
SUSCEPTIBLE TO STATIC CHARGE
COMPLEX PROCESS TECHNOLOGY COMPARED TO NMOS

APPL HIGH DENSITY MEANS IT'S SUITABLE FOR CPU'S, MEMORY, DSP, VLSI
LOW POWER IS GOOD FOR PORTABLE DEVICES

TTL

ADV. WIDESPREAD, INEXPENSIVE, ROBUST, USUALLY FAST ENOUGH
POWER CONSUMPTION NOT VERY FREQUENCY DEPENDENT

DIS-AD LOW DENSITY, DRAWS MORE POWER THAN CMOS AT LOW f
CAUSES NOISE ON POWER LINES, LOW LOW NOISE MARGIN
BEWARE IF $V_{CC} > 5V$

APPLICATIONS EVERYTHING THAT IS ROBUST AND PLUGGED INTO THE WALL. DECREASING IN POPULARITY. I/O DRIVERS, EMBEDDED SYSTEMS

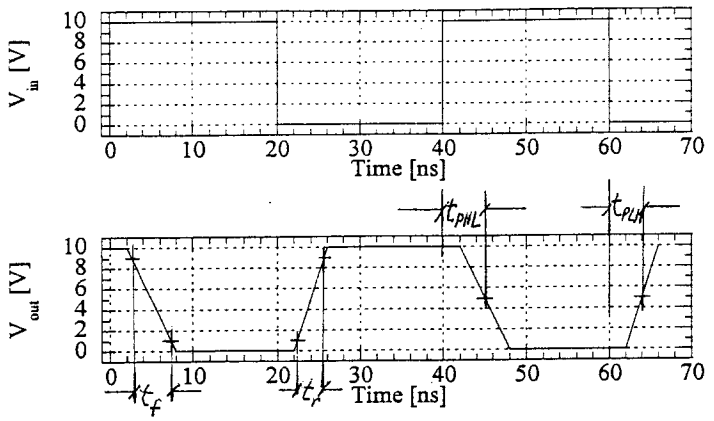
ECL

ADV FAST!!

DIS-AD SMALL LOGIC SWING. INTERFACING TRICKY WITH OTHER LOGIC FAMILIES
SUSCEPTIBLE TO NOISE
CONSUMES LOTS OF POWER!
LOW DENSITY

APPL WHERE SPEED IS CRUCIAL — FAST CPUS

3. A circuit has the following input and output traces:



Please determine the following times and indicate on the graphs above.

1 PT PER

4 PTS EA.

t_r = 3.2 ns = 0.8 · (26ns - 22ns)

t_f = 4.8 ns = 0.8 (8ns - 2ns)

t_{PHL} = 5ns

t_{PLH} = 4ns

What is the frequency of Vin?

5 PTS

$$f = \frac{1}{40ns} = 25MHz$$