

**Instruction set for VBC1
(8 different instructions with 22 variations)**

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Assembly Language Form (ALF) **Transfer Function Form (TFF)**

ADD DR,SR	$DR \leftarrow DR + SR$
ADDI DR,DATA	$DR \leftarrow DR + IR(3:0)$
IN DR	$DR \leftarrow DI(3:0)$
JNZ DR,ADDRESS	$PC \leftarrow IR(3:0)$, if $DR \neq 0$ else $PC \leftarrow PC + 1$
LOADI DR,DATA	$DR \leftarrow IR(3:0)$
MOV DR,SR	$DR \leftarrow SR$
OUT DR	$OP \leftarrow DR$
SR0 DR,SR	$DR \leftarrow 0, SR(3:1)$

Machine Code Form (MCF)

	7:5 OPCODE			DEST Reg	SOURCE Reg			
	7	6	5	4	3	2	1	0
ADD	0	1	0	0/1	0/1	0	0	0
				0 = R0 1 = R1	0 = R0 1 = R1			
ADDI	0	1	1	0/1	D	D	D	D
				0 = R0 1 = R1	3:0 Immediate Data (Source)			
IN	1	0	1	0/1	0	0	0	0
				0 = R0 1 = R1				
JNZ	1	1	1	0/1	A	A	A	A
				0 = R0 1 = R1	3:0 Address (Destination)			
LOADI	0	0	1	0/1	D	D	D	D
				0 = R0 1 = R1	3:0 Immediate Data (Source)			
MOV	0	0	0	0/1	0/1	0	0	0
				0 = R0 1 = R1	0 = R0 1 = R1			
OUT	1	1	0	0/1	0	0	0	0
				0 = R0 1 = R1	SOURCE Reg 3			
SRO	1	0	0	0/1	0/1	0	0	0
				0 = R0 1 = R1	0 = R0 1 = R1			

Complete detailed instruction set for VBC1 in alphabetical order in assembly language form (ALF), transfer function form (TFF), and machine code form (MCF)

The abbreviations in the column Transfer Function Form (TFF) are as follows: DR is Destination Register, SR is Source Register, IR is Instruction Register, DI is Data Input, PC is Program Counter, and OP is Output Port.