Features

- In-System Programmable PROMs for Configuration of Xilinx FPGAs
- Low-Power Advanced CMOS NOR FLASH Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Industrial Temperature Range (−40°C to +85°C)
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply (VCCJ)
- I/O Pins Compatible with Voltage Levels Ranging From 1.5V to 3.3V
- Design Support Using the Xilinx Alliance ISE and Foundation ISE Series Software Packages

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs. Available in 1 to 32 Megabit (Mbit) densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM series includes both the 3.3V XCFxxS PROM and the 1.8V XCFxxP PROM. The XCFxxS version includes 4-Mbit, 2-Mbit, and 1-Mbit PROMs that support Master Serial and Slave Serial FPGA configuration modes (Figure 1, page 2). The XCFxxP version includes 32-Mbit, 16-Mbit, and 8-Mbit PROMs that support Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes (Figure 2, page 2).

A summary of the Platform Flash PROM family members and supported features is shown in Table 1.

Table 1: Platform Flash PROM Features

<table>
<thead>
<tr>
<th>Device</th>
<th>Density</th>
<th>VCCINT</th>
<th>VCCO Range</th>
<th>VCCJ Range</th>
<th>Packages</th>
<th>Program In-system via JTAG</th>
<th>Serial Config.</th>
<th>Parallel Config.</th>
<th>Design Revisioning</th>
<th>Compression</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCF01S</td>
<td>1 Mbit</td>
<td>3.3V</td>
<td>1.8V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO20/VOG20</td>
<td>✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>XCF02S</td>
<td>2 Mbit</td>
<td>3.3V</td>
<td>1.8V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO20/VOG20</td>
<td>✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>XCF04S</td>
<td>4 Mbit</td>
<td>3.3V</td>
<td>1.8V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO20/VOG20</td>
<td>✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>XCF08P</td>
<td>8 Mbit</td>
<td>1.8V</td>
<td>1.5V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO48/VOG48 FS48/FSG48</td>
<td>✓✓ ✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>XCF16P</td>
<td>16 Mbit</td>
<td>1.8V</td>
<td>1.5V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO48/VOG48 FS48/FSG48</td>
<td>✓✓ ✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>XCF32P</td>
<td>32 Mbit</td>
<td>1.8V</td>
<td>1.5V – 3.3V</td>
<td>2.5V – 3.3V</td>
<td>VO48/VOG48 FS48/FSG48</td>
<td>✓✓ ✓✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. With \( CF \) High, a short access time after \( CE \) and \( OE \) are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source, or optionally, for the XCFxxP PROM only, the PROM can be used to drive the FPGA's configuration clock.

The XCFxxP version of the Platform Flash PROM also supports Master SelectMAP and Slave SelectMAP (or Slave Parallel) FPGA configuration modes. When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave SelectMAP Mode, either an external oscillator generates the configuration clock that drives the PROM and the FPGA, or optionally, the XCFxxP PROM can be used to drive the FPGA's configuration clock. With \( BUSY \) Low and \( CF \) High, after \( CE \) and \( OE \) are enabled, data is available on the PROMs DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel /Slave SelectMAP mode.

The XCFxxP version of the Platform Flash PROM provides additional advanced features. A built-in data decompressor supports utilizing compressed PROM files, and design revisioning allows multiple design revisions to be stored on a single PROM or stored across several PROMs. For design revisioning, external pins or internal control bits are used to select the active design revision.

Multiple Platform Flash PROM devices can be cascaded to support the larger configuration files required when targeting larger FPGA devices or targeting multiple FPGAs daisy chained together. When utilizing the advanced features for the XCFxxP Platform Flash PROM, such as design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced XCFxxP features are not enabled, then the cascaded chain can include both XCFxxP and XCFxxS PROMs.
The Platform Flash PROMs are compatible with all of the existing FPGA device families. A reference list of Xilinx FPGAs and the respective compatible Platform Flash PROMs is given in Table 2. A list of Platform Flash PROMs and their capacities is given in Table 3, page 4.

Table 2: Xilinx FPGAs and Compatible Platform Flash PROMs

<table>
<thead>
<tr>
<th>FPGA Configuration</th>
<th>Bitstream Platform Flash PROM(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-5 LX</td>
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</tr>
<tr>
<td>XC5VLX30</td>
<td>8,374,016 XCF08P</td>
</tr>
<tr>
<td>XC5VLX50</td>
<td>12,556,672 XCF16P</td>
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<tr>
<td>XC5VLX85</td>
<td>21,845,632 XCF32P</td>
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<tr>
<td>XC5VLX110</td>
<td>29,124,608 XCF32P</td>
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<tr>
<td>XC5VLX220</td>
<td>53,139,456 XCF32P+XCF32P</td>
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<tr>
<td>XC5VLX330</td>
<td>79,704,832 XCF32P+XCF32P+XCF16P</td>
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<table>
<thead>
<tr>
<th>Virtex-4 LX</th>
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<tbody>
<tr>
<td>XC4VLX15</td>
<td>4,765,568 XCF08P</td>
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<tr>
<td>XC4VLX25</td>
<td>7,819,904 XCF08P</td>
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<tr>
<td>XC4VLX40</td>
<td>12,259,712 XCF16P</td>
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<tr>
<td>XC4VLX60</td>
<td>17,717,632 XCF32P</td>
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<tr>
<td>XC4VLX80</td>
<td>23,291,008 XCF32P</td>
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<tr>
<td>XC4VLX100</td>
<td>30,711,680 XCF32P</td>
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<td>XC4VLX160</td>
<td>40,347,008 XCF32P+XCF08P</td>
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<td>XC4VLX200</td>
<td>51,367,808 XCF32P+XCF32P</td>
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<td>XC4VFX20</td>
<td>7,242,624 XCF08P</td>
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<td>XC4VFX40</td>
<td>14,936,192 XCF16P</td>
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<tr>
<td>XC4VFX60</td>
<td>21,002,880 XCF32P</td>
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<td>XC4VFX100</td>
<td>33,065,408 XCF32P</td>
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<tr>
<td>XC4VFX140</td>
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<td>XC4VXSX55</td>
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<th>Virtex-II Pro X</th>
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<td>XC2VPX20</td>
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<td>XC2VP2</td>
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<td>XC2VP7</td>
<td>4,485,408 XCF08P</td>
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<td>XC2VP20</td>
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<td>XC2VP50</td>
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<tr>
<td>XC2VP100</td>
<td>34,292,768 XCF32P(2)</td>
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Table 3: Xilinx FPGAs and Compatible Platform Flash PROMs (Continued)

<table>
<thead>
<tr>
<th>FPGA Configuration</th>
<th>Bitstream Platform Flash PROM(1)</th>
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<tr>
<td>Virtex-II (3)</td>
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<td>XC2V40</td>
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<td>XC2V80</td>
<td>635,296 XCF01S</td>
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<tr>
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<tr>
<td>XC2V500</td>
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<td>XC2V1000</td>
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<td>XC2V1500</td>
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<tr>
<td>XC2V2000</td>
<td>7,492,000 XCF08P</td>
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<td>XC2V3000</td>
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<td>XC2V4000</td>
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<tr>
<td>XC2V8000</td>
<td>29,063,072 XCF32P</td>
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<table>
<thead>
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<th>Virtex-E</th>
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<td>XCV50E</td>
<td>630,048 XCF01S</td>
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<td>XCV100E</td>
<td>863,840 XCF01S</td>
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<tr>
<td>XCV200E</td>
<td>1,442,016 XCF02S</td>
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<td>XCV3000E</td>
<td>1,875,648 XCF02S</td>
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<tr>
<td>XCV400E</td>
<td>2,693,440 XCF04S</td>
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<td>XCV405E</td>
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<td>XCV600E</td>
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<tr>
<td>XCV812E</td>
<td>6,519,648 XCF08P</td>
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<tr>
<td>XCV1000E</td>
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<td>XCV1600E</td>
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<td>XCV2000E</td>
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<td>XCV2600E</td>
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<td>XCV3200E</td>
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<th>Virtex</th>
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<tr>
<td>XCV50</td>
<td>559,200 XCF01S</td>
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<td>XCV100</td>
<td>781,216 XCF01S</td>
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<tr>
<td>XCV150</td>
<td>1,040,096 XCF01S</td>
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<tr>
<td>XCV200</td>
<td>1,335,840 XCF02S</td>
</tr>
<tr>
<td>XCV300</td>
<td>1,751,808 XCF02S</td>
</tr>
<tr>
<td>XCV400</td>
<td>2,546,048 XCF04S</td>
</tr>
<tr>
<td>XCV600</td>
<td>3,607,968 XCF04S</td>
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<tr>
<td>XCV800</td>
<td>4,715,616 XCF08P</td>
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<tr>
<td>XCV1000</td>
<td>6,127,744 XCF08P</td>
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<table>
<thead>
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<th>Spartan-3E</th>
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<tbody>
<tr>
<td>XC3S100E</td>
<td>581,344 XCF01S</td>
</tr>
<tr>
<td>XC3S250E</td>
<td>1,352,192 XCF02S</td>
</tr>
<tr>
<td>XC3S500E</td>
<td>2,267,136 XCF04S</td>
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</table>
In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 3. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the CEO output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. In-system programming is fully supported across the recommended operating voltage and temperature ranges.

**OE/RESET**

The 1/2/4 Mbit XCFxxS Platform Flash PROMs in-system programming algorithm results in issuance of an internal device reset that causes OE/RESET to pulse Low.

**External Programming**

Xilinx reprogrammable PROMs can also be programmed by the Xilinx MultiPRO Desktop Tool or a third-party device programmer. This provides the added flexibility of using pre-programmed devices with an in-system programmable option for future enhancements and design changes.

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**Table 3: Platform Flash PROM Capacity**

<table>
<thead>
<tr>
<th>Platform Flash PROM</th>
<th>Configuration Bits</th>
<th>Platform Flash PROM</th>
<th>Configuration Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCF01S</td>
<td>1,048,576</td>
<td>XCF08P</td>
<td>8,388,608</td>
</tr>
<tr>
<td>XCF02S</td>
<td>2,097,152</td>
<td>XCF16P</td>
<td>16,777,216</td>
</tr>
<tr>
<td>XCF04S</td>
<td>4,194,304</td>
<td>XCF32P</td>
<td>33,554,432</td>
</tr>
</tbody>
</table>
Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. The XCFxxP PROMs can also be programmed to prevent inadvertent writing via JTAG. Table 4 and Table 5 show the security settings available for the XCFxxS PROM and XCFxxP PROM, respectively.

Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XCFxxS PROM, the read protect security bit is set for the entire device, and resetting the read protect security bit requires erasing the entire device. For the XCFxxP PROM the read protect security bit can be set for individual design revisions, and resetting the read protect bit requires erasing the particular design revision.

Write Protection

The XCFxxP PROM device also allows the user to write protect (or lock) a particular design revision to prevent inadvertent erase or program operations. Once set, the write protect security bit for an individual design revision must be reset (using the UNLOCK command followed by ISC_ERASE command) before an erase or program operation can be performed.

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is compatible with the IEEE 1149.1 boundary-scan standard and the IEEE 1532 in-system configuration standard. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 6, page 6 lists the required and optional boundary-scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

XCFxxS Instruction Register (8 bits wide)

The Instruction Register (IR) for the XCFxxS PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 7, page 6. The instruction capture pattern shifted out of the XCFxxS device includes IR[7:0]. IR[7:5] are reserved bits and are set to a logic 0. The ISC Status field, IR[4], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The Security field, IR[3], contains logic 1 if the device has been programmed with the security option turned on; otherwise, it contains logic 0.

Table 4: XCFxxS Device Data Security Options

<table>
<thead>
<tr>
<th>Read Protect</th>
<th>Read/Verify Inhibited</th>
<th>Program Inhibited</th>
<th>Erase Inhibited</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset (default)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Table 5: XCFxxP Design Revision Data Security Options

<table>
<thead>
<tr>
<th>Read Protect</th>
<th>Write Protect</th>
<th>Read/Verify Inhibited</th>
<th>Program Inhibited</th>
<th>Erase Inhibited</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset (default)</td>
<td>Reset (default)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Reset (default)</td>
<td>Set</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Set</td>
<td>Reset (default)</td>
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<tr>
<td>Set</td>
<td>Set</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Caution! The XCFxxP JTAG TAP pause states are not fully compliant with the JTAG 1149.1 specification. If a temporary pause of a JTAG shift operation is required, then stop the JTAG TCK clock and maintain the JTAG TAP within the JTAG Shift-IR or Shift-DR TAP state. Do not transition the XCFxxP JTAG TAP through the JTAG Pause-IR or Pause-DR TAP state to temporarily pause a JTAG shift operation.
logic 0. IR[2] is unused, and is set to '0'. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

**XCFxxP Instruction Register (16 bits wide)**

The Instruction Register (IR) for the XCFxxP PROM is sixteen bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in *Table 8, page 6*.

The instruction capture pattern shifted out of the XCFxxP device includes IR[15:0]. IR[15:9] are reserved bits and are set to a logic 0. The ISC Error field, IR[8:7], contains a 10 when an ISC operation is a success; otherwise a 01 when an In-System Configuration (ISC) operation fails. The Erase/Program (ER/PROG) Error field, IR[6:5], contains a 10 when an erase or program operation is a success; otherwise a 01 when an erase or program operation fails. The Erase/Program (ER/PROG) Status field, IR[4], contains a logic 0 when the device is busy performing an erase or programming operation; otherwise, it contains a logic 1. The ISC Status field, IR[3], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The DONE field, IR[2], contains logic 1 if the sampled design revision has been successfully programmed; otherwise, a logic 0 indicates incomplete programming. The remaining bits IR[1:0] are set to 01 as defined by IEEE Std. 1149.1.

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**Table 6: Platform Flash PROM Boundary Scan Instructions**

<table>
<thead>
<tr>
<th>Boundary-Scan Command</th>
<th>XCFxxS IR[7:0] (hex)</th>
<th>XCFxxP IR[15:0] (hex)</th>
<th>Instruction Description</th>
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<tbody>
<tr>
<td><strong>Required Instructions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BYPASS</td>
<td>FF</td>
<td>FFFF</td>
<td>Enables BYPASS</td>
</tr>
<tr>
<td>SAMPLE/PRELOAD</td>
<td>01</td>
<td>0001</td>
<td>Enables boundary-scan SAMPLE/PRELOAD operation</td>
</tr>
<tr>
<td>EXTEST</td>
<td>00</td>
<td>0000</td>
<td>Enables boundary-scan EXTEST operation</td>
</tr>
<tr>
<td><strong>Optional Instructions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLAMP</td>
<td>FA</td>
<td>00FA</td>
<td>Enables boundary-scan CLAMP operation</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>FC</td>
<td>00FC</td>
<td>Places all outputs in high-impedance state simultaneously</td>
</tr>
<tr>
<td>IDCODE</td>
<td>FE</td>
<td>00FE</td>
<td>Enables shifting out 32-bit IDCODE</td>
</tr>
<tr>
<td>USERCODE</td>
<td>FD</td>
<td>00FD</td>
<td>Enables shifting out 32-bit USERCODE</td>
</tr>
<tr>
<td><strong>Platform Flash PROM Specific Instructions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONFIG</td>
<td>EE</td>
<td>00EE</td>
<td>Initiates FPGA configuration by pulsing CF pin Low once. (For the XCFxxP this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits.)</td>
</tr>
</tbody>
</table>

**Notes:**
1. For more information see "Initiating FPGA Configuration," page 13.

---

**Table 7: XCFxxS Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reserved</td>
<td>ISC Status</td>
<td>Security</td>
<td>0</td>
<td>01</td>
<td></td>
</tr>
</tbody>
</table>

**Table 8: XCFxxP Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reserved</td>
<td>ISC Error</td>
<td>ER/PROG Error</td>
<td>ER/PROG Status</td>
<td>ISC Status</td>
<td>DONE</td>
<td>01</td>
<td></td>
</tr>
</tbody>
</table>
Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the boundary-scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the boundary-scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See the XCFxxS/XCFxxP Pin Names and Descriptions Tables in the “Pinouts and Pin Descriptions,” page 37 section for the boundary-scan bit order for all connected device pins, or see the appropriate BSDL file for the complete boundary-scan bit order description under the "attribute BOUNDARY_REGISTER" section in the BSDL file. The bit assigned to boundary-scan cell 0 is the LSB in the boundary-scan register, and is the register bit closest to TDO.

Identification Registers

IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG. Table 9 lists the IDCODE register values for the Platform Flash PROMs.

<table>
<thead>
<tr>
<th>Device</th>
<th>IDCODE (1) (hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCF01S</td>
<td>&lt;v&gt;5044093</td>
</tr>
<tr>
<td>XCF02S</td>
<td>&lt;v&gt;5045093</td>
</tr>
<tr>
<td>XCF04S</td>
<td>&lt;v&gt;5046093</td>
</tr>
<tr>
<td>XCF08P</td>
<td>&lt;v&gt;5057093</td>
</tr>
<tr>
<td>XCF16P</td>
<td>&lt;v&gt;5058093</td>
</tr>
<tr>
<td>XCF32P</td>
<td>&lt;v&gt;5059093</td>
</tr>
</tbody>
</table>

Notes:
1. The <v> in the IDCODE field represents the device's revision code (in hex) and may vary.

The IDCODE register has the following binary format:

```
```

where

- v = the die version number
- f = the PROM family code
- a = the specific Platform Flash PROM product ID
- c = the Xilinx manufacturer's ID

The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1.

USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

Customer Code Register

For the XCFxxP Platform Flash PROM, in addition to the USERCODE, a unique 32-byte Customer Code can be assigned to each design revision enabled for the PROM. The Customer Code is set during programming, and is typically used to supply information about the design revision contents. A private JTAG instruction is required to read the Customer Code. If the PROM is blank, or the Customer Code for the selected design revision was not loaded during programming, or if the particular design revision is erased, the Customer Code will contain all ones.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 4, page 8 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.
Table 10 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 10: Test Access Port Timing Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCKMIN</td>
<td>TCK minimum clock period when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>100</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>TMSS</td>
<td>TMS setup time when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>10</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>TMSH</td>
<td>TMS hold time when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>25</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>TDIS</td>
<td>TDI setup time when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>10</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>TDIH</td>
<td>TDI hold time when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>25</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>TDOV</td>
<td>TDO valid delay when $V_{CCJ} = 2.5V$ or $3.3V$</td>
<td>–</td>
<td>30</td>
<td>ns</td>
</tr>
</tbody>
</table>

Additional Features for the XCFxxP

**Internal Oscillator**

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include an optional internal oscillator which can be used to drive the CLKOUT and DATA pins on FPGA configuration interface. The internal oscillator can be enabled during programming the PROM, and the oscillator can be set to either the default frequency or to a slower frequency ("XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source," page 33).

**CLKOUT**

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include the programmable option to enable the CLKOUT signal which allows the PROM to provide a source synchronous clock aligned to the data on the configuration interface. The CLKOUT signal is derived from one of two clock sources: the CLK input pin or the internal oscillator. The input clock source is selected during the PROM programming sequence. Output data is available on the rising edge of CLKOUT.

The CLKOUT signal is enabled during programming, and is active when CE is Low and OE/RESET is High. On CE rising edge transition, if OE/RESET is High and the PROM terminal count has not been reached, then CLKOUT remains active for an additional eight clock cycles before being disabled. On a OE/RESET falling edge transition, CLKOUT is immediately disabled. When disabled, the CLKOUT pin is put into a high-impedance state and should be pulled High externally to provide a known state.

When cascading Platform Flash PROMs with CLKOUT enabled, after completing its data transfer, the first PROM disables CLKOUT and drives the CEO pin enabling the next PROM in the PROM chain. The next PROM will begin driving the CLKOUT signal once that PROM is enabled and data is available for transfer.

During high-speed parallel configuration without compression, the FPGA drives the BUSY signal on the configuration interface. When BUSY is asserted High, the PROMs internal address counter stops incrementing, and the current data value is held on the data outputs. While BUSY is High, the PROM will continue driving the CLKOUT signal to the FPGA, clocking the FPGA’s configuration logic.
When the FPGA deasserts BUSY, indicating that it is ready to receive additional configuration data, the PROM will begin driving new data onto the configuration interface.

### Decompression

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include a built-in data decompressor compatible with Xilinx advanced compression technology. Compressed Platform Flash PROM files are created from the target FPGA bitstream(s) using the iMPACT software. Only Slave Serial and Slave SelectMAP (parallel) configuration modes are supported for FPGA configuration when using a XCFxxP PROM programmed with a compressed bitstream. Compression rates will vary depending on several factors, including the target device family and the target design contents.

The decompression option is enabled during the PROM programming sequence. The PROM decompresses the stored data before driving both clock and data onto the FPGA's configuration interface. If Decompression is enabled, then the Platform Flash clock output pin (CLKOUT) must be used as the clock signal for the configuration interface, driving the target FPGA's configuration clock input pin (CCLK). Either the PROM's CLK input pin or the internal oscillator must be selected as the source for CLKOUT. Any target FPGA connected to the PROM must operate as slave in the configuration chain, with the configuration mode set to Slave Serial mode or Slave SelectMap (parallel) mode.

When decompression is enabled, the CLKOUT signal becomes a controlled clock output with a reduced maximum frequency. When decompressed data is not ready, the CLKOUT pin is put into a high-Z state and must be pulled High externally to provide a known state.

The BUSY input is automatically disabled when decompression is enabled.

### Design Revisioning

Design Revisioning allows the user to create up to four unique design revisions on a single PROM or stored across multiple cascaded PROMs. Design Revisioning is supported for the 8/16/32 Mbit XCFxxP Platform Flash PROMs in both serial and parallel modes. Design Revisioning can be used with compressed PROM files, and also when the CLKOUT feature is enabled. The PROM programming files along with the revision information files (.cfi) are created using the iMPACT software. The .cfi file is required to enable design revision programming in iMPACT.

A single design revision is composed of from 1 to \( n \) 8-Mbit memory blocks. If a single design revision contains less than 8 Mbits of data, then the remaining space is padded with all ones. A larger design revision can span several 8-Mbit memory blocks, and any space remaining in the last 8-Mbit memory block is padded with all ones.

- A single 32-Mbit PROM contains four 8-Mbit memory blocks, and can therefore store up to four separate design revisions: one 32-Mbit design revision, two 16-Mbit design revisions, three 8-Mbit design revisions, four 8-Mbit design revisions, and so on.
- Because of the 8-Mbit minimum size requirement for each revision, a single 16-Mbit PROM can only store up to two separate design revisions: one 16-Mbit design revision, one 8-Mbit design revision, or two 8-Mbit design revisions.
- A single 8-Mbit PROM can store only one 8-Mbit design revision.

Larger design revisions can be split over several cascaded PROMs. For example, two 32-Mbit PROMs can store up to four separate design revisions: one 64-Mbit design revision, two 32-Mbit design revisions, three 16-Mbit design revisions, four 16-Mbit design revisions, and so on. When cascading one 16-Mbit PROM and one 8-Mbit PROM, there are 24 Mbits of available space, and therefore up to three separate design revisions can be stored: one 24-Mbit design revision, two 8-Mbit design revisions, or three 8-Mbit design revisions.

See Figure 5, page 10 for a few basic examples of how multiple revisions can be stored. The design revision partitioning is handled automatically during file generation in iMPACT.

During the PROM file creation, each design revision is assigned a revision number:

- Revision 0 = '00'
- Revision 1 = '01'
- Revision 2 = '10'
- Revision 3 = '11'

After programming the Platform Flash PROM with a set of design revisions, a particular design revision can be selected using the external REV_SEL[1:0] pins or using the internal programmable design revision control bits. The EN_EXT_SEL pin determines if the external pins or internal bits are used to select the design revision. When EN_EXT_SEL is Low, design revision selection is controlled by the external Revision Select pins, REV_SEL[1:0]. When EN_EXT_SEL is High, design revision selection is controlled by the internal programmable Revision Select control bits. During power up, the design revision selection inputs (pins or control bits) are sampled internally. After power up, the design revision selection inputs are sampled again when any of the following events occur:

- On the rising edge of CE
- On the falling edge of OE/RESET (when CE is Low)
- On the rising edge of CF (when CE is Low)
- When reconfiguration is initiated by using the JTAG CONFIG instruction.

The data from the selected design revision is then presented on the FPGA configuration interface.
PROM to FPGA Configuration Mode and Connections Summary

The FPGA's I/O, logical functions, and internal interconnections are established by the configuration data contained in the FPGA's bitstream. The bitstream is loaded into the FPGA either automatically upon power up, or on command, depending on the state of the FPGA's mode pins. Xilinx Platform Flash PROMs are designed to download directly to the FPGA configuration interface. FPGA configuration modes which are supported by the XCFxxS Platform Flash PROMs include: Master Serial and Slave Serial. FPGA configuration modes which are supported by the XCFxxP Platform Flash PROMs include: Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP. Below is a short summary of the supported FPGA configuration modes. See the respective FPGA data sheet for device configuration details, including which configuration modes are supported by the targeted FPGA device.

FPGA Master Serial Mode

In Master Serial mode, the FPGA automatically loads the configuration bitstream in bit-serial form from external memory synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA's DIN input pin a short time before each rising edge of the FPGA's internally generated CCLK signal.

Typically, a wide range of frequencies can be selected for the FPGA's internally generated CCLK which always starts...
at a slow default frequency. The FPGA’s bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master Serial configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master Serial Configuration Mode (Figure 6, page 14):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The CE output of a PROM drives the CE input of the next PROM in a daisy chain (if any).
- The OE/RESET pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM CE input can be driven from the DONE pin. The CE input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary Icc active supply current (“DC Characteristics Over Operating Conditions,” page 26).
- The PROM CF pin is typically connected to the FPGA’s PROG_B (or PROGRAM) input. For the XCfxxP only, the CF pin is a bidirectional pin. If the XCFxxP CF pin is not connected to the FPGA’s PROG_B (or PROGRAM) input, then the pin should be tied High.

**FPGA Slave Serial Mode**

In Slave Serial mode, the FPGA loads the configuration bitstream in bit-serial form from external memory synchronized by an externally supplied clock. Upon power-up or reconfiguration, the FPGA’s mode select pins are used to select the Slave Serial configuration mode. Slave Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM’s internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA’s DIN input pin a short time before each rising edge of the externally provided CCLK.

Connecting the FPGA device to the configuration PROM for Slave Serial Configuration Mode (Figure 7, page 15):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The PROM CLKOUT (for XCfxxP only) or an external clock source drives the FPGA’s CCLK input.
- The CE output of a PROM drives the CE input of the next PROM in a daisy chain (if any).
- The OE/RESET pins of all PROMs are connected to the INIT_B (or INIT) pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM CE input can be driven from the DONE pin. The CE input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary Icc active supply current (“DC Characteristics Over Operating Conditions,” page 26).
- The PROM CF pin is typically connected to the FPGA’s PROG_B (or PROGRAM) input. For the XCFxxP only, the CF pin is a bidirectional pin. If the XCfxxP CF pin is not connected to the FPGA’s PROG_B (or PROGRAM) input, then the pin should be tied High.

**Serial Daisy Chain**

Multiple FPGAs can be daisy-chained for serial configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the FPGA’s DOUT pin. Typically the data on the DOUT pin changes on the falling edge of CCLK, although for some devices the DOUT pin changes on the rising edge of CCLK. Consult the respective device data sheets for detailed information on a particular FPGA device. For the XCFxxP only, the CF pin is a bidirectional pin. If the XCFxxP CF pin is not connected to the FPGA’s PROG_B (or PROGRAM) input, then the pin should be tied High.

**FPGA Master SelectMAP (Parallel) Mode (XCFxxP PROM Only)**

In Master SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA’s mode select pins are used to select the Master SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGA’s Chip Select, Write, and BUSY pins must be correctly controlled to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM’s internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be set up at the FPGA’s [D0..D7] input pins a short time before each rising edge of the FPGA’s...
The Master SelectMAP configuration interface is clocked by the FPGA's internal oscillator. Typically, a wide range of frequencies can be selected for the internally generated CCLK which always starts at a slow default frequency. The FPGA's bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master SelectMAP configuration sequence. The desired CCLK frequency is selected during bitstream generation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained using the persist option.

Connecting the FPGA device to the configuration PROM for Master SelectMAP (Parallel) Configuration Mode (Figure 9, page 17):

- The DATA outputs of the PROM(s) drive the [D0..D7] input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The CEO output of a PROM drives the CE input of the next PROM in a daisy chain (if any).
- The OE/RESET pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM CE input can be driven from the DONE pin. The CE input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary ICC active supply current (“DC Characteristics Over Operating Conditions,” page 26).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output. This connection assures that the next data transition for the PROM is delayed until the FPGA is ready for the next configuration data byte.
- The PROM CF pin is typically connected to the FPGA's PROG_B (or PROGRAM) input. For the XCFxxP only, the CF pin is a bidirectional pin. If the XCFxxP CF pin is not connected to the FPGA's PROG_B (or PROGRAM) input, then the pin should be tied High.

FPGA Slave SelectMAP (Parallel) Mode (XCFxxP PROM Only)

In Slave SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by an externally supplied configuration clock (CCLK). Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGA's Chip Select, Write, and BUSY pins must be correctly controlled to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be set up at the FPGA's [D0..D7] input pins a short time before each rising edge of the provided CCLK. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. An external data source or external pull-down resistors must be used to enable the FPGA's active Low Chip Select (CS or CS_B) and Write (WRITE or RDWR_B) signals to enable the FPGA's SelectMAP configuration process.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained using the persist option.

Connecting the FPGA device to the configuration PROM for Slave SelectMAP (Parallel) Configuration Mode (Figure 10, page 18):

- The DATA outputs of the PROM(s) drives the [D0..D7] inputs of the lead FPGA device.
- The PROM CLKOUT (for XCFxxP only) or an external clock source drives the FPGA's CCLK input.
- The CEO output of a PROM drives the CE input of the next PROM in a daisy chain (if any).
- The OE/RESET pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM CE input can be driven from the DONE pin. The CE input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary ICC active supply current (“DC Characteristics Over Operating Conditions,” page 26).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output. This connection assures that the next data transition for the PROM is delayed until the FPGA is ready for the next configuration data byte.
• The PROM CF pin is typically connected to the FPGA's PROG_B (or PROGRAM) input. For the XCFxxP only, the CF pin is a bidirectional pin. If the XCFxxP CF pin is not connected to the FPGA's PROG_B (or PROGRAM) input, then the pin should be tied High.

**FPGA SelectMAP (Parallel) Device Chaining (XCFxxP PROM Only)**

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode and be made to start up simultaneously. To configure multiple devices in this way, wire the individual CCLK, DONE, INIT, Data ([D0..D7]), Write (WRITE or RDWR_B), and BUSY pins of all the devices in parallel. If all devices are to be configured with the same bitstream, readback is not being used, and the CCLK frequency selected does not require the use of the BUSY signal, the CS_B pins can be connected to a common line so all of the devices are configured simultaneously (Figure 10, page 18).

With additional control logic, the individual devices can be loaded separately by asserting the CS_B pin of each device in turn and then enabling the appropriate configuration data. The PROM can also store the individual bitstreams for each FPGA for SelectMAP configuration in separate design revisions. When design revisioning is utilized, additional control logic can be used to select the appropriate bitstream by asserting the EN_EXT_SEL pin, and using the REV_SEL[1:0] pins to select the required bitstream, while asserting the CS_B pin for the FPGA the bitstream is targeting (Figure 13, page 21).

For clocking the parallel configuration chain, either the first FPGA in the chain can be set to Master SelectMAP, generating the CCLK, with the remaining devices set to Slave SelectMAP, or all the FPGA devices can be set to Slave SelectMAP and an externally generated clock can be used to drive the configuration interface. Again, the respective device data sheets should be consulted for detailed information on a particular FPGA device, including which configuration modes are supported by the targeted FPGA device.

**Cascading Configuration PROMs**

When configuring multiple FPGAs in a serial daisy chain, configuring multiple FPGAs in a SelectMAP parallel chain, or configuring a single FPGA requiring a larger configuration bitstream, cascaded PROMs provide additional memory (Figure 8, page 16, Figure 11, page 19, Figure 12, page 20, and Figure 13, page 21). Multiple Platform Flash PROMs can be concatenated by using the CEO output to drive the CE input of the downstream device. The clock signal and the data outputs of all Platform Flash PROMs in the chain are interconnected. After the last data from the first PROM is read, the first PROM asserts its CEO output Low and drives its outputs to a high-impedance state. The second PROM recognizes the Low level on its CE input and immediately enables its outputs.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/RESET pin goes Low or CE goes High.

When utilizing the advanced features for the XCFxxP Platform Flash PROM, including the clock output (CLKOUT) option, decompression option, or design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced features are not used, then cascaded PROM chains can contain both XCFxxP and XCFxxS PROMs.

**Initiating FPGA Configuration**

The options for initiating FPGA configuration via the Platform Flash PROM include:

- Automatic configuration on power up
- Applying an external PROG_B (or PROGRAM) pulse
- Applying the JTAG CONFIG instruction

Following the FPGA's power-on sequence or the assertion of the PROG_B (or PROGRAM) pin the FPGA's configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROG_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a CF pin that can be tied to the FPGA's PROG_B pin. Executing the CONFIG instruction through JTAG pulses the CF output Low once for 300-500 ns, resetting the FPGA and initiating configuration. The Impact software can issue the JTAG CONFIG command to initiate FPGA configuration by setting the “Load FPGA” option.

When using the XCFxxP Platform Flash PROM with design revisioning enabled, the CF pin should always be connected to the PROG_B (or PROGRAM) pin on the FPGA to ensure that the current design revision selection is sampled when the FPGA is reset. The XCFxxP PROM samples the current design revision selection from the external REV_SEL pins or the internal programmable Revision Select bits on the rising edge of CF. When the JTAG CONFIG command is executed, the XCFxxP will sample the new design revision selection before initiating the FPGA configuration sequence. When using the XCFxxP Platform Flash PROM without design revisioning, if the CF pin is not connected to the FPGA PROG_B (or PROGRAM) pin, then the XCFxxP CF pin must be tied High.
**Figure 6: Configuring in Master Serial Mode**

Notes:
1. For Mode pin connections and DONE pin pull-up, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. For the XCFxxS the CF pin is an output pin. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.
Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally—for the XCFxxP Platform Flash PROM only—the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then CLKOUT must be tied to a 4.7 kΩ resistor pulled up to VCCO.
4. For the XCFxxS the CF pin is an output pin. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

Figure 7: Configuring in Slave Serial Mode
Figure 8: Configuring Multiple Devices in Master/Slave Serial Mode

Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. For the XCFxxS the CF pin is an output pin. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.
Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. CS_B (or CS) and RDWR_B (or WRITE) must be either driven Low or pulled down externally. One option is shown.
4. The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.
5. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

**Figure 9:** Configuring in Master SelectMAP Mode
Figure 10: Configuring in Slave SelectMAP Mode

Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. CS_B (or CS) and RDWR_B (or WRITE) must be either driven Low or pulled down externally. One option is shown.
4. The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.
5. In Slave SelectMAP mode, the configuration interface can be clocked by an external oscillator, or, optionally, the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then CLKOUT must be tied to a 4.7 kΩ resistor pulled up to VCCO.
6. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.
Figure 11: Configuring Multiple Devices with Identical Patterns in Master/Slave SelectMAP Mode

Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. CS_B (or CS) and RDWR_B (or WRITE) must be either driven Low or pulled down externally. One option is shown.
4. The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.
5. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.
**Figure 12:** Configuring Multiple Devices with Design Revisioning in Slave Serial Mode

Notes:
1. For mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally the CLKOUT signal can be used to drive the FPGA’s configuration clock (CCLK). If the XCFxxP PROM’s CLKOUT signal is used, then CLKOUT must be tied to a 4.7 kΩ resistor pulled up to \( V_{CCO} \).
4. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to \( V_{CCO} \) via a 4.7 kΩ pull-up resistor.
Figure 13: Configuring Multiple Devices with Design Revisioning in Slave SelectMAP Mode

Notes:
1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
2. For compatible voltages, refer to the appropriate data sheet.
3. RDWR_B (or WRITE) must be either driven Low or pulled down externally. One option is shown.
4. The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.
5. In Slave SelectMAP mode, the configuration interface can be clocked by an external oscillator, or optionally the CLKOUT signal can be used to drive the FPGA’s configuration clock (CCLK). If the XCFxxP PROM’s CLKOUT signal is used, then it must be tied to a 4.7 kΩ resistor pulled up to VCCO.
6. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROGB, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.
Reset and Power-On Reset Activation

At power up, the device requires the $V_{CCINT}$ power supply to monotonically rise to the nominal operating voltage within the specified $V_{CCINT}$ rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/RESET is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/RESET release is delayed ($T_{OER}$ minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/RESET pin is connected to an external 4.7kΩ pull-up resistor and also to the target FPGA’s INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/RESET pin Low. When OE/RESET is released, the FPGA’s INIT pin is pulled High allowing the FPGA’s configuration sequence to begin. If the power drops below the power-down threshold ($V_{CCPD}$), the PROM resets and OE/RESET is again held Low until after the POR threshold is reached. OE/RESET polarity is not programmable. These power-up requirements are shown graphically in Figure 14, page 22.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/RESET is asserted (Low) or CE is deasserted (High). The address counter is reset, CEO is driven High, and the remaining outputs are placed in a high-impedance state.

Notes:
1. The XCFxxS PROM only requires $V_{CCINT}$ to rise above its POR threshold before releasing OE/RESET.
2. The XCFxxP PROM requires both $V_{CCINT}$ and $V_{CCO}$ to rise above their POR thresholds and for $V_{CCO}$ to reach the recommended operating voltage level before releasing OE/RESET.

I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V-tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The core power supply ($V_{CCINT}$), JTAG pin power supply ($V_{CCJ}$), output power supply ($V_{CCO}$), and external 3V CMOS I/O signals can be applied in any order.

Additionally, for the XCFxxS PROM only, when $V_{CCO}$ is supplied at 2.5V or 3.3V and $V_{CCINT}$ is supplied at 3.3V, the I/Os are 5V-tolerant. This allows 5V CMOS signals to connect directly to the inputs on a powered XCFxxS PROM without damage. Failure to power the PROM correctly while supplying a 5V input signal may result in damage to the XCFxxS device.

Standby Mode

The PROM enters a low-power standby mode whenever CE is deasserted (High). In standby mode, the address counter is reset, CEO is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the OE/RESET input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

When using the FPGA DONE signal to drive the PROM CE pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330Ω
pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and is also connected to the PROM CE pin to enable low-power standby mode, then an external buffer should be used to drive the LED circuit to ensure valid transitions on the PROM's CE pin. If low-power standby mode is not required for the PROM, then the CE pin should be connected to ground.

Table 11: Truth Table for XCFxxS PROM Control Inputs

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Internal Address</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE/RESET</td>
<td>CE</td>
<td>DATA</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>If address &lt; TC(2) : increment</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If address = TC(2) : don't change</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>Held reset</td>
</tr>
<tr>
<td>X(1)</td>
<td>High</td>
<td>Held reset</td>
</tr>
</tbody>
</table>

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value.

Table 12: Truth Table for XCFxxP PROM Control Inputs

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Internal Address</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE/RESET</td>
<td>CE</td>
<td>CF</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High</td>
<td>Low</td>
<td>↑ X(1) Reset(4)</td>
</tr>
<tr>
<td>Low</td>
<td>Low</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>High</td>
<td>X</td>
</tr>
</tbody>
</table>

Notes:
1. X = don’t care.
2. TC = Terminal Count = highest address value.
3. For the XCFxxP with Design Revisioning enabled, EA = end address (last address in the selected design revision).
4. For the XCFxxP with Design Revisioning enabled, Reset = address reset to the beginning address of the selected bank. If Design Revisioning is not enabled, then Reset = address reset to address 0.
5. The BUSY input is only enabled when the XCFxxP is programmed for parallel data output and decompression is not enabled.
DC Electrical Characteristics

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCINT</td>
<td>Internal supply voltage relative to GND</td>
<td>–0.5 to +4.0</td>
<td>–0.5 to +2.7</td>
<td>V</td>
</tr>
<tr>
<td>VCCO</td>
<td>I/O supply voltage relative to GND</td>
<td>–0.5 to +4.0</td>
<td>–0.5 to +4.0</td>
<td>V</td>
</tr>
<tr>
<td>VCCJ</td>
<td>JTAG I/O supply voltage relative to GND</td>
<td>–0.5 to +4.0</td>
<td>–0.5 to +4.0</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage with respect to GND</td>
<td>VCCO &lt; 2.5V</td>
<td>–0.5 to +3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCCO ≥ 2.5V</td>
<td>–0.5 to +5.5</td>
<td>V</td>
</tr>
<tr>
<td>VTS</td>
<td>Voltage applied to High-Z output</td>
<td>VCCO &lt; 2.5V</td>
<td>–0.5 to +3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCCO ≥ 2.5V</td>
<td>–0.5 to +5.5</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature (ambient)</td>
<td>–65 to +150</td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature</td>
<td>+125</td>
<td>+125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
3. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at www.xilinx.com.

Supply Voltage Requirements for Power-On Reset and Power-Down

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TVCC</td>
<td>VCCINT rise time from 0V to nominal voltage(2)</td>
<td>0.2</td>
<td>50</td>
<td>ms</td>
</tr>
<tr>
<td>VCCPOR</td>
<td>POR threshold for the VCCINT supply</td>
<td>1</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>TOER</td>
<td>OE/RESET release delay following POR(3)</td>
<td>0.5</td>
<td>3</td>
<td>ms</td>
</tr>
<tr>
<td>VCCPD</td>
<td>Power-down threshold for VCCINT supply</td>
<td>–</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>TRST</td>
<td>Time required to trigger a device reset</td>
<td>10</td>
<td>–</td>
<td>ms</td>
</tr>
</tbody>
</table>

Notes:
1. VCCINT, VCCO, and VCCJ supplies may be applied in any order.
2. At power up, the device requires the VCCINT power supply to monotonically rise to the nominal operating voltage within the specified TVCC rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 14, page 22.
3. If the VCCINT and VCCO supplies do not reach their respective recommended operating conditions before the OE/RESET pin is released, then the configuration data from the PROM will not be available at the recommended threshold levels. The configuration sequence must be delayed until both VCCINT and VCCO have reached their recommended operating conditions.
# Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>V\text{CCINT}</td>
<td>Internal voltage supply</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
</tr>
<tr>
<td>V\text{CCO}</td>
<td>Supply voltage for output drivers</td>
<td>3.3V Operation</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V Operation</td>
<td>2.3</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8V Operation</td>
<td>1.7</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5V Operation</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>V\text{CCJ}</td>
<td>Supply voltage for JTAG output drivers</td>
<td>3.3V Operation</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V Operation</td>
<td>2.3</td>
<td>2.5</td>
</tr>
<tr>
<td>V\text{IL}</td>
<td>Low-level input voltage</td>
<td>3.3V Operation</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V Operation</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8V Operation</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5V Operation</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>V\text{IH}</td>
<td>High-level input voltage</td>
<td>3.3V Operation</td>
<td>2.0</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V Operation</td>
<td>1.7</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8V Operation</td>
<td>70% V\text{CCO}</td>
<td>3.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5V Operation</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>T\text{IN}</td>
<td>Input signal transition time(^{(1)})</td>
<td>–</td>
<td>–</td>
<td>500</td>
</tr>
<tr>
<td>V\text{O}</td>
<td>Output voltage</td>
<td>0</td>
<td>–</td>
<td>V\text{CCO}</td>
</tr>
<tr>
<td>T\text{A}</td>
<td>Operating ambient temperature</td>
<td>–40</td>
<td>–</td>
<td>85</td>
</tr>
</tbody>
</table>

**Notes:**
1. Input signal transition time measured between 10% V\text{CCO} and 90% V\text{CCO}.

# Quality and Reliability Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>T\text{DR}</td>
<td>Data retention</td>
<td>20</td>
<td>–</td>
<td>Years</td>
</tr>
<tr>
<td>N\text{PE}</td>
<td>Program/erase cycles (Endurance)</td>
<td>20,000</td>
<td>–</td>
<td>Cycles</td>
</tr>
<tr>
<td>V\text{ESD}</td>
<td>Electrostatic discharge (ESD)</td>
<td>2,000</td>
<td>–</td>
<td>Volts</td>
</tr>
</tbody>
</table>
## DC Characteristics Over Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Test Conditions</td>
<td>Min</td>
<td>Max</td>
<td>Test Conditions</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>High-level output voltage for 3.3V outputs</td>
<td>( I_{OH} = -4 \text{ mA} )</td>
<td>2.4</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>High-level output voltage for 2.5V outputs</td>
<td>( I_{OH} = -500 \mu\text{A} )</td>
<td>( V_{CCO} - 0.4 )</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>High-level output voltage for 1.8V outputs</td>
<td>( I_{OH} = -50 \mu\text{A} )</td>
<td>( V_{CCO} - 0.4 )</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>High-level output voltage for 1.5V outputs</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Low-level output voltage for 3.3V outputs</td>
<td>( I_{OL} = 4 \text{ mA} )</td>
<td>–</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Low-level output voltage for 2.5V outputs</td>
<td>( I_{OL} = 500 \mu\text{A} )</td>
<td>–</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Low-level output voltage for 1.8V outputs</td>
<td>( I_{OL} = 50 \mu\text{A} )</td>
<td>–</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Low-level output voltage for 1.5V outputs</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>( I_{CCINT} )</td>
<td>Internal voltage supply current, active mode</td>
<td>33 MHz</td>
<td>–</td>
<td>10</td>
</tr>
<tr>
<td>( I_{CCO(1)} )</td>
<td>Output driver supply current, active serial mode</td>
<td>33 MHz</td>
<td>–</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Output driver supply current, active parallel mode</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>( I_{CCJ} )</td>
<td>JTAG supply current, active mode</td>
<td>Note (2)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>( I_{CCINTS} )</td>
<td>Internal voltage supply current, standby mode</td>
<td>Note (3)</td>
<td>–</td>
<td>5</td>
</tr>
<tr>
<td>( I_{CCOS} )</td>
<td>Output driver supply current, standby mode</td>
<td>Note (3)</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>( I_{CCJS} )</td>
<td>JTAG supply current, standby mode</td>
<td>Note (3)</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>( I_{ILJ} )</td>
<td>JTAG pins TMS, TDI, and TDO pull-up current</td>
<td>( V_{CCJ} = \text{max} ) ( V_{IN} = \text{GND} )</td>
<td>–</td>
<td>100</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input leakage current</td>
<td>( V_{CCINT} = \text{max} ) ( V_{CCO} = \text{max} ) ( V_{IN} = \text{GND} ) or ( V_{CCO} )</td>
<td>–10</td>
<td>10</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Input and output High-Z leakage current</td>
<td>( V_{CCINT} = \text{max} ) ( V_{CCO} = \text{max} ) ( V_{IN} = \text{GND} ) or ( V_{CCO} )</td>
<td>–10</td>
<td>10</td>
</tr>
<tr>
<td>( I_{ILP} )</td>
<td>Source current through internal pull-ups on EN_EXT_SEL, REV_SEL0, REV_SEL1</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>( I_{IHLP} )</td>
<td>Sink current through internal pull-down on BUSY</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input capacitance</td>
<td>( V_{IN} = \text{GND} ) ( f = 1.0 \text{ MHz} )</td>
<td>–</td>
<td>8</td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>Output capacitance</td>
<td>( V_{IN} = \text{GND} ) ( f = 1.0 \text{ MHz} )</td>
<td>–</td>
<td>14</td>
</tr>
</tbody>
</table>

**Notes:**

1. Output driver supply current specification based on no load conditions.
2. TDI/TMS/TCK non-static (active).
3. CE High, OE Low, and TMS/TDI/TCK static.
### AC Electrical Characteristics

#### AC Characteristics Over Operating Conditions

**XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Units</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
</tr>
</thead>
</table>
| \( T_{HC} \) | CF hold time to guarantee design revision selection is sampled when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \) | 300 | 300 | ns |
| \( T_{CF} \) | CF hold time to guarantee design revision selection is sampled when \( V_{CCO} = 1.8\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | 300 | 300 | ns |
| \( T_{OE} \) | CF to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | – | – | 25 | ns |
| \( T_{CE} \) | OE/RESET to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | – | 10 | – | 25 | ns |
| \( T_{CAC} \) | CF to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | – | 15 | – | 25 | ns |
| \( T_{DF} \) | CLK to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | – | 30 | – | 25 | ns |
| \( T_{CV} \) | Data hold from \( CE \), \( OE/RESET \), \( CLK \), or CF when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \)
| | \( V_{CCO} = 1.8\text{V} \) | 0 | – | 5 | – | ns |

---

**Notes:**
- \( THCF \): CF hold time to guarantee design revision selection is sampled when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \).
- \( THCE \): CF hold time to guarantee design revision selection is sampled when \( V_{CCO} = 1.8\text{V} \).
- \( TOE \): OE/RESET to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \).
- \( TCE \): CE to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \).
- \( TDF \): CLK to data delay when \( V_{CCO} = 3.3\text{V} \) or \( 2.5\text{V} \).
- \( TOE \): OE/RESET to data delay when \( V_{CCO} = 1.8\text{V} \).
- \( TCE \): CE to data delay when \( V_{CCO} = 1.8\text{V} \).
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>T(_{DF})</td>
<td>CE or OE/RESET to data float delay(^{(2)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>–</td>
<td>25</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CE or OE/RESET to data float delay(^{(2)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>–</td>
<td>30</td>
<td>–</td>
</tr>
<tr>
<td>T(_{CYC})</td>
<td>Clock period(^{(6)}) (serial mode) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>30</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>Clock period(^{(6)}) (serial mode) when (V_{CCO} = 1.8,\text{V})</td>
<td>67</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>Clock period(^{(6)}) (parallel mode) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>–</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>Clock period(^{(6)}) (parallel mode) when (V_{CCO} = 1.8,\text{V})</td>
<td>–</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td>T(_{LC})</td>
<td>CLK Low time(^{(3)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>10</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>CLK Low time(^{(3)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>15</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td>T(_{HC})</td>
<td>CLK High time(^{(3)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>10</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>CLK High time(^{(3)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>15</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td>T(_{SCE})</td>
<td>CE setup time to CLK (guarantees proper counting)(^{(3)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>20</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>CE setup time to CLK (guarantees proper counting)(^{(3)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>30</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td>T(_{HCE})</td>
<td>CE hold time (guarantees counters are reset)(^{(5)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>250</td>
<td>–</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>CE hold time (guarantees counters are reset)(^{(5)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>250</td>
<td>–</td>
<td>2000</td>
</tr>
<tr>
<td>T(_{HOE})</td>
<td>OE/RESET hold time (guarantees counters are reset)(^{(6)}) when (V_{CCO} = 3.3,\text{V or 2.5,V})</td>
<td>250</td>
<td>–</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>OE/RESET hold time (guarantees counters are reset)(^{(6)}) when (V_{CCO} = 1.8,\text{V})</td>
<td>250</td>
<td>–</td>
<td>2000</td>
</tr>
<tr>
<td>T(_{SB})</td>
<td>BUSY setup time to CLK when (V_{CCO} = 3.3,\text{V or 2.5,V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>BUSY setup time to CLK when (V_{CCO} = 1.8,\text{V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>12</td>
</tr>
<tr>
<td>T(_{HB})</td>
<td>BUSY hold time to CLK when (V_{CCO} = 3.3,\text{V or 2.5,V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>BUSY hold time to CLK when (V_{CCO} = 1.8,\text{V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>8</td>
</tr>
<tr>
<td>T(_{SXT})</td>
<td>EN(<em>{\text{EXT SEL}}) setup time to CF, CE or OE/RESET when (V</em>{CCO} = 3.3,\text{V or 2.5,V})(^{(6)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>EN(<em>{\text{EXT SEL}}) setup time to CF, CE or OE/RESET when (V</em>{CCO} = 1.8,\text{V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td>T(_{HXT})</td>
<td>EN(<em>{\text{EXT SEL}}) hold time from CF, CE or OE/RESET when (V</em>{CCO} = 3.3,\text{V or 2.5,V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>EN(<em>{\text{EXT SEL}}) hold time from CF, CE or OE/RESET when (V</em>{CCO} = 1.8,\text{V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td>T(_{SRV})</td>
<td>REV(<em>{\text{SEL}}) setup time to CF, CE or OE/RESET when (V</em>{CCO} = 3.3,\text{V or 2.5,V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>REV(<em>{\text{SEL}}) setup time to CF, CE or OE/RESET when (V</em>{CCO} = 1.8,\text{V})(^{(8)})</td>
<td>–</td>
<td>–</td>
<td>300</td>
</tr>
</tbody>
</table>
### Symbol Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>REV_SEL hold time from CF, CE or OE/RESET when V&lt;sub&gt;CCO&lt;/sub&gt; = 3.3V or 2.5V&lt;sup&gt;(8)&lt;/sup&gt;</td>
<td>–</td>
<td>–</td>
<td>300</td>
<td>– ns</td>
</tr>
<tr>
<td>REV_SEL hold time from CF, CE or OE/RESET when V&lt;sub&gt;CCO&lt;/sub&gt; = 1.8V&lt;sup&gt;(8)&lt;/sup&gt;</td>
<td>–</td>
<td>–</td>
<td>300</td>
<td>– ns</td>
</tr>
</tbody>
</table>

**Notes:**

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. All AC parameters are measured with V<sub>IL</sub> = 0.0V and V<sub>IH</sub> = 3.0V.
4. If T<sub>HCE</sub> High < 2 µs, T<sub>CE</sub> = 2 µs.
5. If T<sub>HOE</sub> Low < 2 µs, T<sub>OE</sub> = 2 µs.
6. This is the minimum possible T<sub>CYC</sub>. Actual T<sub>CYC</sub> = T<sub>CAC</sub> + FPGA Data setup time. Example: With the XCF32P in serial mode with V<sub>CCO</sub> at 3.3V, if FPGA data setup time = 15 ns, then the actual T<sub>CYC</sub> = 25 ns + 15 ns = 40 ns.
7. Guaranteed by design; not tested.
8. CF, EN_EXT_SEL, REV_SEL[1:0], and BUSY are inputs for the XCFxxP PROM only.
9. When JTAG CONFIG command is issued, PROM will drive CF Low for at least the T<sub>HCF</sub> minimum.
XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF08P, XCF16P, XCF32P</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>THRCE</td>
<td>CF hold time to guarantee design revision selection is sampled when $V_{CCO} = 3.3V$ or $2.5V^{(11)}$</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>CF hold time to guarantee design revision selection is sampled when $V_{CCO} = 1.8V^{(11)}$</td>
<td>300</td>
</tr>
<tr>
<td>TCFS</td>
<td>CF to data delay when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CF to data delay when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
<tr>
<td>TOE</td>
<td>OE/RESET to data delay$^{(6)}$ when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>OE/RESET to data delay$^{(6)}$ when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
<tr>
<td>TCE</td>
<td>CE to data delay$^{(5)}$ when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CE to data delay$^{(5)}$ when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
<tr>
<td>TEOH</td>
<td>Data hold from CE, OE/RESET, or CF when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>Data hold from CE, OE/RESET, or CF when $V_{CCO} = 1.8V$</td>
<td>5</td>
</tr>
<tr>
<td>TDF</td>
<td>CE or OE/RESET to data float delay$^{(2)}$ when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CE or OE/RESET to data float delay$^{(2)}$ when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
<tr>
<td>TOECEF</td>
<td>OE/RESET to CLKOUT float delay$^{(2)}$ when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>OE/RESET to CLKOUT float delay$^{(2)}$ when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
<tr>
<td>TCECEF</td>
<td>CE to CLKOUT float delay$^{(2)}$ when $V_{CCO} = 3.3V$ or $2.5V$</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CE to CLKOUT float delay$^{(2)}$ when $V_{CCO} = 1.8V$</td>
<td>–</td>
</tr>
</tbody>
</table>

Note: 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>T_CYCO</td>
<td>Clock period (serial mode) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>30</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Clock period (serial mode) when $V_{CCO} = 1.8\text{V}$</td>
<td>30</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Clock period (parallel mode) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Clock period (parallel mode) when $V_{CCO} = 1.8\text{V}$</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td>T_LC</td>
<td>CLK Low time (serial mode) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CLK Low time (serial mode) when $V_{CCO} = 1.8\text{V}$</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td>T_HC</td>
<td>CLK High time (parallel mode) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CLK High time (parallel mode) when $V_{CCO} = 1.8\text{V}$</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td>T_CECC</td>
<td>CE hold time (guarantees counters are reset) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>2000</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CE hold time (guarantees counters are reset) when $V_{CCO} = 1.8\text{V}$</td>
<td>2000</td>
<td>–</td>
</tr>
<tr>
<td>T_OECC</td>
<td>OE/RESET hold time (guarantees counters are reset) when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>2000</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>OE/RESET hold time (guarantees counters are reset) when $V_{CCO} = 1.8\text{V}$</td>
<td>2000</td>
<td>–</td>
</tr>
<tr>
<td>T_SB</td>
<td>BUSY setup time to CLKOUT when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>BUSY setup time to CLKOUT when $V_{CCO} = 1.8\text{V}$</td>
<td>12</td>
<td>–</td>
</tr>
<tr>
<td>T_HB</td>
<td>BUSY hold time to CLKOUT when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>8</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>BUSY hold time to CLKOUT when $V_{CCO} = 1.8\text{V}$</td>
<td>8</td>
<td>–</td>
</tr>
<tr>
<td>T_CLKO</td>
<td>CLK input to CLKOUT output delay when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>–</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>CLK input to CLKOUT output delay when $V_{CCO} = 1.8\text{V}$</td>
<td>–</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>CLK input to CLKOUT output delay when $V_{CCO} = 3.3\text{V}$ or 2.5V with decompression</td>
<td>–</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>CLK input to CLKOUT output delay when $V_{CCO} = 1.8\text{V}$ with decompression</td>
<td>–</td>
<td>35</td>
</tr>
<tr>
<td>T_CECC</td>
<td>CE to CLKOUT delay when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>0</td>
<td>2 CLK cycles</td>
</tr>
<tr>
<td></td>
<td>CE to CLKOUT delay when $V_{CCO} = 1.8\text{V}$</td>
<td>0</td>
<td>2 CLK cycles</td>
</tr>
<tr>
<td>T_OECC</td>
<td>OE/RESET to CLKOUT delay when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>0</td>
<td>2 CLK cycles</td>
</tr>
<tr>
<td></td>
<td>OE/RESET to CLKOUT delay when $V_{CCO} = 1.8\text{V}$</td>
<td>0</td>
<td>2 CLK cycles</td>
</tr>
<tr>
<td>T_CFFC</td>
<td>CF to CLKOUT delay when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>0</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td>CF to CLKOUT delay when $V_{CCO} = 1.8\text{V}$</td>
<td>0</td>
<td>TBD</td>
</tr>
<tr>
<td>T_CCDD</td>
<td>CLKOUT to data delay when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>CLKOUT to data delay when $V_{CCO} = 1.8\text{V}$</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td>T_DDC</td>
<td>Data setup time to CLKOUT when $V_{CCO} = 3.3\text{V}$ or 2.5V with decompression</td>
<td>5</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Data setup time to CLKOUT when $V_{CCO} = 1.8\text{V}$ with decompression</td>
<td>5</td>
<td>–</td>
</tr>
<tr>
<td>T_COH</td>
<td>Data hold from CLKOUT when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when $V_{CCO} = 1.8\text{V}$</td>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when $V_{CCO} = 3.3\text{V}$ or 2.5V with decompression</td>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when $V_{CCO} = 1.8\text{V}$ with decompression</td>
<td>3</td>
<td>–</td>
</tr>
<tr>
<td>T_SXT</td>
<td>$\text{EN_EXT_SEL}$ setup time to CF, CE, or OE/RESET when $V_{CCO} = 3.3\text{V}$ or 2.5V</td>
<td>300</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>$\text{EN_EXT_SEL}$ setup time to CF, CE, or OE/RESET when $V_{CCO} = 1.8\text{V}$</td>
<td>300</td>
<td>–</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>XCF08P, XCF16P, XCF32P</td>
<td>Units</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>THXT</td>
<td>EN_EXT_SEL hold time from CF, CE, or OE/RESET when V_CCO = 3.3V or 2.5V</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>EN_EXT_SEL hold time from CF, CE, or OE/RESET when V_CCO = 1.8V</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>T_SRV</td>
<td>REV_SEL setup time to CF, CE, or OE/RESET when V_CCO = 3.3V or 2.5V</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>REV_SEL setup time to CF, CE, or OE/RESET when V_CCO = 1.8V</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>T_HRV</td>
<td>REV_SEL hold time from CF, CE, or OE/RESET when V_CCO = 3.3V or 2.5V</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>REV_SEL hold time from CF, CE, or OE/RESET when V_CCO = 1.8V</td>
<td>300</td>
<td>ns</td>
</tr>
</tbody>
</table>

Notes:
1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_IL = 0.0V and V_IH = 3.0V.
5. If THCE High < 2 µs, T_CE = 2 µs.
6. If T_HOE Low < 2 µs, T_OE = 2 µs.
7. This is the minimum possible T_CYCO. Actual T_CYCO = T_CCDD + FPGA Data setup time. Example: With the XCF32P in serial mode with V_CCO at 3.3V, if FPGA Data setup time = 15 ns, then the actual T_CYCO = 25 ns + 15 ns = 40 ns.
8. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled will increase if decompression is enabled.
9. Slower CLK frequency option may be required to meet the FPGA data sheet setup time.
10. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT will toggle at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7kΩ pull-up to V_CCO.
11. When JTAG CONFIG command is issued, PROM will drive CF Low for at least the T_HCF minimum.
### XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source

#### Symbol Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{HC}$</td>
<td>CF hold time to guarantee design revision selection is sampled when $V_{CCO} = 3.3V$ or 2.5V(^{(12)})</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>$T_{HF}$</td>
<td>CF hold time to guarantee design revision selection is sampled when $V_{CCO} = 1.8V$(^{(12)})</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>$T_C$</td>
<td>CF to data delay when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>TBD</td>
</tr>
<tr>
<td>$T_{OE}$</td>
<td>OE/RESET to data delay(^{(6)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>$T_{OE}$</td>
<td>OE/RESET to data delay(^{(6)}) when $V_{CCO} = 1.8V$</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>$T_{CE}$</td>
<td>CE to data delay(^{(5)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>$T_{CE}$</td>
<td>CE to data delay(^{(5)}) when $V_{CCO} = 1.8V$</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>$T_{EOH}$</td>
<td>Data hold from CE, OE/RESET, or CF when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>5</td>
<td>–</td>
</tr>
<tr>
<td>$T_{DF}$</td>
<td>CE or OE/RESET to data float delay(^{(2)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>45</td>
</tr>
<tr>
<td>$T_{OE}$</td>
<td>CE or OE/RESET to data float delay(^{(2)}) when $V_{CCO} = 1.8V$</td>
<td>–</td>
<td>45</td>
</tr>
<tr>
<td>$T_{OE}$</td>
<td>OE/RESET to CLKOUT float delay(^{(2)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>TBD</td>
</tr>
<tr>
<td>$T_{OE}$</td>
<td>OE/RESET to CLKOUT float delay(^{(2)}) when $V_{CCO} = 1.8V$</td>
<td>–</td>
<td>TBD</td>
</tr>
<tr>
<td>$T_{DE}$</td>
<td>CE to CLKOUT float delay(^{(2)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>–</td>
<td>TBD</td>
</tr>
<tr>
<td>$T_{DE}$</td>
<td>CE to CLKOUT float delay(^{(2)}) when $V_{CCO} = 1.8V$</td>
<td>–</td>
<td>TBD</td>
</tr>
<tr>
<td>$T_{HCE}$</td>
<td>CE hold time (guarantees counters are reset)(^{(5)}) when $V_{CCO} = 3.3V$ or 2.5V</td>
<td>2000</td>
<td>–</td>
</tr>
<tr>
<td>$T_{HCE}$</td>
<td>CE hold time (guarantees counters are reset)(^{(5)}) when $V_{CCO} = 1.8V$</td>
<td>2000</td>
<td>–</td>
</tr>
</tbody>
</table>

**Note:** 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.

---

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<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_HOE</td>
<td>OE/RESET hold time (guarantees counters are reset) ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>2000 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>OE/RESET hold time (guarantees counters are reset) ( v_{CCO} = 1.8V )</td>
<td>2000 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_SB</td>
<td>BUSY setup time to CLKOUT when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>12 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>BUSY setup time to CLKOUT when ( v_{CCO} = 1.8V )</td>
<td>12 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_HB</td>
<td>BUSY hold time to CLKOUT when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>8 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>BUSY hold time to CLKOUT when ( v_{CCO} = 1.8V )</td>
<td>8 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_CEC</td>
<td>CE to CLKOUT delay when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>0 1 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CE to CLKOUT delay when ( v_{CCO} = 1.8V )</td>
<td>0 1 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td>T_OEC</td>
<td>OE/RESET to CLKOUT delay when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>0 1 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OE/RESET to CLKOUT delay when ( v_{CCO} = 1.8V )</td>
<td>0 1 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td>T_CFC</td>
<td>CF to CLKOUT delay when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>0 TBD –</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>CF to CLKOUT delay when ( v_{CCO} = 1.8V )</td>
<td>0 TBD –</td>
<td>–</td>
</tr>
<tr>
<td>T_CDD</td>
<td>CLKOUT to data delay when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>– 30 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLKOUT to data delay when ( v_{CCO} = 1.8V )</td>
<td>– 30 ns</td>
<td></td>
</tr>
<tr>
<td>T_DDC</td>
<td>Data setup time to CLKOUT when ( v_{CCO} = 3.3V ) or 2.5V with decompression</td>
<td>5 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data setup time to CLKOUT when ( v_{CCO} = 1.8V ) with decompression(8)(11)</td>
<td>5 ns</td>
<td></td>
</tr>
<tr>
<td>T_COH</td>
<td>Data hold from CLKOUT when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>3 – ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when ( v_{CCO} = 1.8V )</td>
<td>3 – ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when ( v_{CCO} = 3.3V ) or 2.5V with decompression(11)</td>
<td>3 – ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data hold from CLKOUT when ( v_{CCO} = 1.8V ) with decompression(11)</td>
<td>3 – ns</td>
<td></td>
</tr>
<tr>
<td>T_SXT</td>
<td>EN_EXT_SEL setup time to CF, CE, or OE/RESET when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>EN_EXT_SEL setup time to CF, CE, or OE/RESET when ( v_{CCO} = 1.8V )</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_HXT</td>
<td>EN_EXT_SEL hold time from CF, CE, or OE/RESET when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>EN_EXT_SEL hold time from CF, CE, or OE/RESET when ( v_{CCO} = 1.8V )</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_SRV</td>
<td>REV_SEL setup time to CF, CE, or OE/RESET when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>REV_SEL setup time to CF, CE, or OE/RESET when ( v_{CCO} = 1.8V )</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>T_HRV</td>
<td>REV_SEL hold time from CF, CE, or OE/RESET when ( v_{CCO} = 3.3V ) or 2.5V</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>REV_SEL hold time from CF, CE, or OE/RESET when ( v_{CCO} = 1.8V )</td>
<td>300 – ns</td>
<td>ns</td>
</tr>
<tr>
<td>F_F</td>
<td>CLKOUT default (fast) frequency(9)</td>
<td>12.5 25 MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>CLKOUT default (fast) frequency with decompression(11)</td>
<td>12.5 25 MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>XCF08P, XCF16P, XCF32P</td>
<td>Units</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>-------------------------</td>
<td>-------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>$F_S$</td>
<td>CLKOUT alternate (slower) frequency$^{(10)}$</td>
<td>12.5</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>CLKOUT alternate (slower) frequency with decompression$^{(11)}$</td>
<td>6</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Notes:
1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$.
5. If $T_{HCE\; High} < 2 \mu s$, $T_{CE} = 2 \mu s$.
6. If $T_{HOE\; Low} < 2 \mu s$, $T_{OE} = 2 \mu s$.
7. The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled will increase if decompression is enabled.
8. Slower CLK frequency option may be required to meet the FPGA data sheet setup time.
9. Typical CLKOUT default (fast) period = 25 ns (40 MHz)
10. Typical CLKOUT alternate (slower) period = 50 ns (20 MHz)
11. When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT will toggle at $\frac{1}{2}$ the source clock frequency (either $\frac{1}{2}$ the selected internal clock frequency or $\frac{1}{2}$ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7k$\Omega$ pull-up to $V_{CCO}$.
12. When JTAG CONFIG command is issued, PROM will drive $CF$ Low for at least the $T_{HCF}$ minimum.
## AC Characteristics Over Operating Conditions When Cascading

### Symbol and Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>XCF01S, XCF02S, XCF04S</th>
<th>XCF08P, XCF16P, XCF32P</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCDF</td>
<td>CLK to output float delay(^{(2,3)}) when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>25</td>
<td>–</td>
</tr>
<tr>
<td>TCDF</td>
<td>CLK to output float delay(^{(2,3)}) when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td>TOCK</td>
<td>CLK to CEO delay(^{(3,5)}) when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>20</td>
<td>–</td>
</tr>
<tr>
<td>TOCK</td>
<td>CLK to CEO delay(^{(3,5)}) when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td>TOCE</td>
<td>CE to CEO delay(^{(3,6)}) when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>20</td>
<td>–</td>
</tr>
<tr>
<td>TOCE</td>
<td>CE to CEO delay(^{(3,6)}) when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td>TOOE</td>
<td>OE/RESET to CEO delay(^{(3)}) when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>20</td>
<td>–</td>
</tr>
<tr>
<td>TOOE</td>
<td>OE/RESET to CEO delay(^{(3)}) when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>35</td>
<td>–</td>
</tr>
<tr>
<td>TCOCE</td>
<td>CLKOUT to CEO delay when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>TCOCE</td>
<td>CLKOUT to CEO delay when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>TCODF</td>
<td>CLKOUT to output float delay when (V_{CCO} = 2.5V) or (3.3V)</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>TCODF</td>
<td>CLKOUT to output float delay when (V_{CCO} = 1.8V)</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

### Notes:

1. AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with \(V_{IL} = 0.0V\) and \(V_{IH} = 3.0V\).
5. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins are set to persist as configuration pins, the minimum period is increased based on the CLK to CEO and CE to data propagation delays:
   - \(T_{CYC}^{\text{minimum}} = T_{OCE} + T_{CE} + \text{FPGA Data setup time}\)
   - \(T_{CYC}^{\text{maximum}} = T_{OCE} + T_{CE}\)
6. For cascaded PROMs, if the FPGA's dual-purpose configuration data pins become general I/O pins after configuration; to allow for the disable to propagate to the cascaded PROMs and to avoid contention on the data lines following configuration, the minimum period is increased based on the CE to CEO and CE to data propagation delays:
   - \(T_{CYC}^{\text{minimum}} = T_{OCE} + T_{CE}\)
   - \(T_{CYC}^{\text{maximum}} = T_{OCE} + T_{CE}\)
Pinouts and Pin Descriptions

The XCFxxS Platform Flash PROM is available in the VO20 and VOG20 packages. The XCFxxP Platform Flash PROM is available in the VO48, VOG48, FS48, and FSG48 packages.

Notes:
1. VO20/VOG20 denotes a 20-pin (TSSOP) Plastic Thin Shrink Small Outline Package
3. FS48/FSG48 denotes a 48-pin (TFBGA) Plastic Thin Fine Pitch Ball Grid Array (0.8 mm pitch).

XCFxxS Pinouts and Pin Descriptions

Table 13: XCFxxS Pin Names and Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Boundary Scan Order</th>
<th>Boundary Scan Function</th>
<th>Pin Description</th>
<th>20-pin TSSOP (VO20/VOG20)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>4</td>
<td>Data Out</td>
<td>D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Output Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>0</td>
<td>Data In</td>
<td>Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, CE is Low, and OE/RESET is High.</td>
<td>3</td>
</tr>
<tr>
<td>OE/RESET</td>
<td>20</td>
<td>Data In</td>
<td>Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>19</td>
<td>Data Out</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>Output Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CE</td>
<td>15</td>
<td>Data In</td>
<td>Chip Enable Input. When CE is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.</td>
<td>10</td>
</tr>
<tr>
<td>CF</td>
<td>22</td>
<td>Data Out</td>
<td>Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>21</td>
<td>Output Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CEO</td>
<td>12</td>
<td>Data Out</td>
<td>Chip Enable Output. Chip Enable Output (CEO) is connected to the CE input of the next PROM in the chain. This output is Low when CE is Low and OE/RESET input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. CEO returns to High when OE/RESET goes Low or CE goes High.</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Output Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMS</td>
<td></td>
<td>Mode Select</td>
<td>JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 KΩ resistive pull-up to VCCJ to provide a logic 1 to the device if the pin is not driven.</td>
<td>5</td>
</tr>
<tr>
<td>TCK</td>
<td></td>
<td>Clock</td>
<td>JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.</td>
<td>6</td>
</tr>
<tr>
<td>TDI</td>
<td></td>
<td>Data In</td>
<td>JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 KΩ resistive pull-up to VCCJ to provide a logic 1 to the device if the pin is not driven.</td>
<td>4</td>
</tr>
<tr>
<td>TDO</td>
<td></td>
<td>Data Out</td>
<td>JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 KΩ resistive pull-up to VCCJ to provide a logic 1 to the system if the pin is not driven.</td>
<td>17</td>
</tr>
<tr>
<td>VCCINT</td>
<td></td>
<td>+3.3V Supply. Positive 3.3V supply voltage for internal logic.</td>
<td></td>
<td>18</td>
</tr>
</tbody>
</table>
Table 13: XCFxxS Pin Names and Descriptions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Boundary Scan Order</th>
<th>Boundary Scan Function</th>
<th>Pin Description</th>
<th>20-pin TSSOP (VO20/VOG20)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCO</td>
<td></td>
<td>+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>VCCJ</td>
<td></td>
<td>+3.3V or 2.5V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>DNC</td>
<td></td>
<td>Do not connect. (These pins must be left unconnected.)</td>
<td>2, 9, 12, 14, 15, 16</td>
<td></td>
</tr>
</tbody>
</table>

XCFxxS VO20/VOG20 Pinout Diagram

![VO20/VOG20 Pinout Diagram](image)

Figure 15: VO20/VOG20 Pinout Diagram (Top View) with Pin Names
### XCFxxP Pinouts and Pin Descriptions

**VXCFxxP O48/VOG48 and FS48/FSG48 Pin Names and Descriptions**

Table 14 provides a list of the pin names and descriptions for the XCFxxP 48-pin VO48/VOG48 and 48-pin FS48/FSG48 packages.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Boundary Scan Order</th>
<th>Boundary Scan Function</th>
<th>Pin Description</th>
<th>48-pin TSOP (VO48/VOG48)</th>
<th>48-pin TFBGA (FS48/FSG48)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>28</td>
<td>Data Out</td>
<td>D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.</td>
<td>28</td>
<td>H6</td>
</tr>
<tr>
<td></td>
<td>27</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>26</td>
<td>Data Out</td>
<td>D1 is the DATA output pin to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode.</td>
<td>29</td>
<td>H5</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>24</td>
<td>Data Out</td>
<td>D2-D7 are the DATA output pins to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode.</td>
<td>32</td>
<td>E5</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>Output Enable</td>
<td>The D0 output is set to a high-impedance state during ISPEN (when not clamped).</td>
<td>33</td>
<td>D5</td>
</tr>
<tr>
<td>D3</td>
<td>22</td>
<td>Data Out</td>
<td>The D1-D7 outputs are set to a high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. The D1-D7 pins can be left unconnected when the PROM is used in serial mode.</td>
<td>33</td>
<td>D5</td>
</tr>
<tr>
<td>D4</td>
<td>21</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>Data Out</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>19</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>Data Out</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>17</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>16</td>
<td>Data Out</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>01</td>
<td>Data In</td>
<td>Configuration Clock Input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected. CE is Low, OE/RESET is High, BUSY is Low (parallel mode only), and CF is High.</td>
<td>12</td>
<td>B3</td>
</tr>
<tr>
<td>OE/RESET</td>
<td>04</td>
<td>Data In</td>
<td>Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.</td>
<td>11</td>
<td>A3</td>
</tr>
<tr>
<td></td>
<td>03</td>
<td>Data Out</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>02</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CE</td>
<td>00</td>
<td>Data In</td>
<td>Chip Enable Input. When CE is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high-impedance state.</td>
<td>13</td>
<td>B4</td>
</tr>
<tr>
<td>CF</td>
<td>11</td>
<td>Data In</td>
<td>Configuration Pulse (Open-Drain I/O). As an output, this pin allows the JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain signal that is pulsed Low by the JTAG CONFIG command. As an input, on the rising edge of CF, the current design revision selection is sampled and the internal address counter is reset to the start address for the selected revision. If unused, the CF pin must be pulled High using an external 4.7 KΩ pull-up to $V_{CCO}$.</td>
<td>6</td>
<td>D1</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>Data Out</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>09</td>
<td>Output Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 14: XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Boundary Scan Order</th>
<th>Boundary Scan Function</th>
<th>Pin Description</th>
<th>48-pin TSOP (VO48/VOG48)</th>
<th>48-pin TFBGA (FS48/FSG48)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEO</td>
<td>06</td>
<td>Data Out</td>
<td>Chip Enable Output. Chip Enable Output (CEO) is connected to the CE input of the next PROM in the chain. This output is Low when CE is Low and OE/RESET input is High. AND the internal address counter has been incremented beyond its Terminal Count (TC) value. CEO returns to High when OE/RESET goes Low or CE goes High.</td>
<td>10</td>
<td>D2</td>
</tr>
<tr>
<td>EN_EXT_SEL</td>
<td>31</td>
<td>Data In</td>
<td>Enable External Selection Input. When this pin is Low, design revision selection is controlled by the Revision Select pins. When this pin is High, design revision selection is controlled by the internal programmable Revision Select control bits. EN_EXT_SEL has an internal 50KΩ resistive pull-up to VCCO to provide a logic 1 to the device if the pin is not driven.</td>
<td>25</td>
<td>H4</td>
</tr>
<tr>
<td>REV_SEL0</td>
<td>30</td>
<td>Data In</td>
<td>Revision Select[1:0] Inputs. When the EN_EXT_SEL is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmable Revision Select control bits. The Revision Select[1:0] inputs have an internal 50 KΩ resistive pull-up to VCCO to provide a logic 1 to the device if the pins are not driven.</td>
<td>26</td>
<td>G3</td>
</tr>
<tr>
<td>REV_SEL1</td>
<td>29</td>
<td>Data In</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BUSY</td>
<td>12</td>
<td>Data In</td>
<td>Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50 KΩ resistive pull-down to GND to provide a logic 0 to the device if the pin is not driven.</td>
<td>5</td>
<td>C1</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>08</td>
<td>Data Out</td>
<td>Configuration Clock Output. An internal Programmable control bit enables the CLKOUT signal, which is sourced from either the internal oscillator or the CLK input pin. Each rising edge of the selected clock source increments the internal address counter if data is available, CE is Low, and OE/RESET is High. Output data is available on the rising edge of CLKOUT. CLKOUT is disabled if CE is High or OE/RESET is Low. If decompression is enabled, CLKOUT is parked High when decompressed data is not ready. When CLKOUT is disabled, the CLKOUT pin is put into a high-Z state. If CLKOUT is used, then it must be pulled High externally using a 4.7 KΩ pull-up to VCCO.</td>
<td>9</td>
<td>C2</td>
</tr>
<tr>
<td>TMS</td>
<td>07</td>
<td>Output Enable</td>
<td>Mode Select</td>
<td>JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 KΩ resistive pull-up to VCCO to provide a logic 1 to the device if the pin is not driven.</td>
<td></td>
</tr>
<tr>
<td>TCK</td>
<td>05</td>
<td>Clock</td>
<td>JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.</td>
<td>20</td>
<td>H3</td>
</tr>
<tr>
<td>TDI</td>
<td>04</td>
<td>Data In</td>
<td>JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 KΩ resistive pull-up to VCCO to provide a logic 1 to the device if the pin is not driven.</td>
<td>19</td>
<td>G1</td>
</tr>
<tr>
<td>TDO</td>
<td>03</td>
<td>Data Out</td>
<td>JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 KΩ resistive pull-up to VCCO to provide a logic 1 to the system if the pin is not driven.</td>
<td>22</td>
<td>E6</td>
</tr>
<tr>
<td>VCCINT</td>
<td></td>
<td></td>
<td>+1.8V Supply. Positive 1.8V supply voltage for internal logic.</td>
<td>4, 15, 34</td>
<td>B1, E1, G6</td>
</tr>
</tbody>
</table>
### Table 14: XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) (Continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Boundary Scan Order</th>
<th>Boundary Scan Function</th>
<th>Pin Description</th>
<th>48-pin TSOP (VO48/VOG48)</th>
<th>48-pin TFBGA (FS48/FSG48)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCO</td>
<td></td>
<td></td>
<td>+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.</td>
<td>8, 30, 38, 45</td>
<td>B2, C6, D6, G5</td>
</tr>
<tr>
<td>VCCJ</td>
<td></td>
<td></td>
<td>+3.3V or 2.5V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.</td>
<td>24</td>
<td>H2</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td></td>
<td>Ground</td>
<td>2, 7, 17, 23, 31, 36, 46</td>
<td>A1, A2, B6, F1, F5, F6, H1</td>
</tr>
<tr>
<td>DNC</td>
<td></td>
<td></td>
<td>Do Not Connect. (These pins must be left unconnected.)</td>
<td>1, 3, 14, 16, 18, 35, 37, 39, 40, 41, 42</td>
<td>A4, C3, C4, D3, D4, E3, E4, F2, F3, F4, G2</td>
</tr>
</tbody>
</table>

### XCFxxP VO48/VOG48 Pinout Diagram

Figure 16: VO48/VOG48 Pinout Diagram (Top View) with Pin Names
### XCFxxP FS48/FSG48 Pin Names

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>E1</td>
<td>VCCINT</td>
</tr>
<tr>
<td>A2</td>
<td>GND</td>
<td>E2</td>
<td>TMS</td>
</tr>
<tr>
<td>A3</td>
<td>OE/RESET</td>
<td>E3</td>
<td>DNC</td>
</tr>
<tr>
<td>A4</td>
<td>DNC</td>
<td>E4</td>
<td>DNC</td>
</tr>
<tr>
<td>A5</td>
<td>D6</td>
<td>E5</td>
<td>D2</td>
</tr>
<tr>
<td>A6</td>
<td>D7</td>
<td>E6</td>
<td>TDO</td>
</tr>
<tr>
<td>B1</td>
<td>VCCINT</td>
<td>F1</td>
<td>GND</td>
</tr>
<tr>
<td>B2</td>
<td>VCCO</td>
<td>F2</td>
<td>DNC</td>
</tr>
<tr>
<td>B3</td>
<td>CLK</td>
<td>F3</td>
<td>DNC</td>
</tr>
<tr>
<td>B4</td>
<td>CE</td>
<td>F4</td>
<td>DNC</td>
</tr>
<tr>
<td>B5</td>
<td>D5</td>
<td>F5</td>
<td>GND</td>
</tr>
<tr>
<td>B6</td>
<td>GND</td>
<td>F6</td>
<td>GND</td>
</tr>
<tr>
<td>C1</td>
<td>BUSY</td>
<td>G1</td>
<td>TDI</td>
</tr>
<tr>
<td>C2</td>
<td>CLKOUT</td>
<td>G2</td>
<td>DNC</td>
</tr>
<tr>
<td>C3</td>
<td>DNC</td>
<td>G3</td>
<td>REV_SEL0</td>
</tr>
<tr>
<td>C4</td>
<td>DNC</td>
<td>G4</td>
<td>REV_SEL1</td>
</tr>
<tr>
<td>C5</td>
<td>D4</td>
<td>G5</td>
<td>VCCO</td>
</tr>
<tr>
<td>C6</td>
<td>VCCO</td>
<td>G6</td>
<td>VCCINT</td>
</tr>
<tr>
<td>D1</td>
<td>CF</td>
<td>H1</td>
<td>GND</td>
</tr>
<tr>
<td>D2</td>
<td>CEO</td>
<td>H2</td>
<td>VCCJ</td>
</tr>
<tr>
<td>D3</td>
<td>DNC</td>
<td>H3</td>
<td>TCK</td>
</tr>
<tr>
<td>D4</td>
<td>DNC</td>
<td>H4</td>
<td>EN_EXT_SEL</td>
</tr>
<tr>
<td>D5</td>
<td>D3</td>
<td>H5</td>
<td>D1</td>
</tr>
<tr>
<td>D6</td>
<td>VCCO</td>
<td>H6</td>
<td>D0</td>
</tr>
</tbody>
</table>

### XCFxxP FS48/FSG48 Pinout Diagram

![FS48/FSG48 Pinout Diagram (Top View)](ds121_01_071604)

Figure 17: FS48/FSG48 Pinout Diagram (Top View)
Ordering Information

### XCF04S VO20 C

- **Device Number:** XCF01S, XCF02S, XCF04S
- **Package Type:** VO20 = 20-pin TSSOP Package
- **Operating Range/Processing:** C = (TA = –40°C to +85°C)
- **Marking Information:**
  - V = 20-pin TSSOP Package (VO20)
  - VG = 20-pin TSSOP Package, Pb-free (VOG20)

### XCF32P FS48 C

- **Device Number:** XCF08P, XCF16P, XCF32P
- **Package Type:** VO48 = 48-pin TSOP Package
- **Operating Range/Processing:** C = (TA = –40°C to +85°C)
- **Marking Information:**
  - VO48 = 48-pin TSOP Package
  - VOG48 = 48-pin TSOP Package, Pb-free
  - FS48 = 48-pin TFBGA Package
  - FSG48 = 48-pin TFBGA Package, Pb-free

Valid Ordering Combinations

<table>
<thead>
<tr>
<th>XCF01SVO20 C</th>
<th>XCF08PVO48 C</th>
<th>XCF08PFS48 C</th>
<th>XCF01SVOG20 C</th>
<th>XCF08PVOG48 C</th>
<th>XCF08PFSG48 C</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCF02SVO20 C</td>
<td>XCF16PVO48 C</td>
<td>XCF16PFS48 C</td>
<td>XCF02SVOG20 C</td>
<td>XCF16PVOG48 C</td>
<td>XCF16PFSG48 C</td>
</tr>
<tr>
<td>XCF04SVO20 C</td>
<td>XCF32PVO48 C</td>
<td>XCF32PFS48 C</td>
<td>XCF04SVOG20 C</td>
<td>XCF32PVOG48 C</td>
<td>XCF32PFSG48 C</td>
</tr>
</tbody>
</table>

Marking Information

<table>
<thead>
<tr>
<th>Device Number</th>
<th>XCF04S-V</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCF01S</td>
<td>Package Type</td>
</tr>
<tr>
<td>XCF02S</td>
<td>V = 20-pin TSSOP Package (VO20)</td>
</tr>
<tr>
<td>XCF04S</td>
<td>VG = 20-pin TSSOP Package, Pb-free (VOG20)</td>
</tr>
<tr>
<td>XCF08P</td>
<td>VO48 = 48-pin TSOP Package (VO48)</td>
</tr>
<tr>
<td>XCF16P</td>
<td>VOG48 = 48-pin TSOP Package, Pb-free (VOG48)</td>
</tr>
<tr>
<td>XCF32P</td>
<td>F48 = 48-pin TFBGA Package (FS48)</td>
</tr>
<tr>
<td></td>
<td>FG48 = 48-pin TFBGA Package, Pb-free (FSG48)</td>
</tr>
</tbody>
</table>

**Operating Range/Processing:** C = (TA = –40°C to +85°C)
# Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>04/29/03</td>
<td>1.0</td>
<td>Xilinx Initial Release.</td>
</tr>
<tr>
<td>06/03/03</td>
<td>1.1</td>
<td>Made edits to all pages.</td>
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<tr>
<td>11/05/03</td>
<td>2.0</td>
<td>Major revision.</td>
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<tr>
<td>11/18/03</td>
<td>2.1</td>
<td>Pinout corrections as follows:</td>
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<td></td>
<td></td>
<td>• Table 14:</td>
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<td></td>
<td></td>
<td>♦ For VO48 package, removed 38 from VCCINT and added it to VCCO.</td>
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<tr>
<td></td>
<td></td>
<td>♦ For FS48 package, removed pin D6 from VCCINT and added it to VCCO.</td>
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<td></td>
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<td>• Table 15 (FS48 package):</td>
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<td>♦ For pin D6, changed name from VCCINT to VCCO.</td>
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<td>♦ For pin A4, changed name from GND to DNC.</td>
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<td>• Figure 16 (VO48 package): For pin 38, changed name from VCCINT to VCCO.</td>
</tr>
<tr>
<td>12/15/03</td>
<td>2.2</td>
<td>• Added specification (4.7kΩ) for recommended pull-up resistor on OE/RESET pin to section &quot;Reset and Power-On Reset Activation,&quot; page 22.</td>
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<tr>
<td></td>
<td></td>
<td>• Added paragraph to section &quot;Standby Mode,&quot; page 22, concerning use of a pull-up resistor and/or buffer on the DONE pin.</td>
</tr>
<tr>
<td>05/07/04</td>
<td>2.3</td>
<td>• Section &quot;Features,&quot; page 1: Added package styles and 33 MHz configuration speed limit to itemized features.</td>
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<td></td>
<td>• Section &quot;Description,&quot; page 1 and following: Added State conditions for CF and BUSY to the descriptive text.</td>
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<td></td>
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<td>• Table 2, page 3: Updated Virtex-II configuration bitstream sizes.</td>
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<td></td>
<td>• Section &quot;Design Revisioning,&quot; page 9: Rewritten.</td>
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<td></td>
<td>• Section &quot;PROM to FPGA Configuration Mode and Connections Summary,&quot; page 10 and following, five instances: Added instruction to tie CF High if it is not tied to the FPGA's PROG_B (PROGRAM) input.</td>
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<td>• Figure 6, page 14, through Figure 13, page 21: Added footnote indicating the directionality of the CF pin in each configuration.</td>
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<td>• Section &quot;I/O Input Voltage Tolerance and Power Sequencing,&quot; page 22: Rewritten.</td>
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<td>• Table 12, page 23: Added CF column to truth table, and added an additional row to document the Low state of CF.</td>
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<td>• Section &quot;Absolute Maximum Ratings,&quot; page 24: Revised VIN and VTS for 'P' devices.</td>
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<td>• Section &quot;Supply Voltage Requirements for Power-On Reset and Power-Down,&quot; page 24:</td>
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<td></td>
<td>♦ Revised footnote callout number on T_OER from Footnote (4) to Footnote (3).</td>
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<td>♦ Added Footnote (2) callout to TVCC.</td>
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<td></td>
<td>• Section &quot;Recommended Operating Conditions,&quot; page 25:</td>
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<tr>
<td></td>
<td></td>
<td>♦ Added Typical (Typ) parameter columns and parameters for VCCINT and VCCO/VCCJ.</td>
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<tr>
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<td>♦ Added 1.5V operation parameter row to VIL and VIH, 'P' devices.</td>
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<tr>
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<td></td>
<td>♦ Revised V_HH Min, 2.5V operation, from 2.0V to 1.7V.</td>
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<td></td>
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<td>♦ Added parameter row T_IN and Max parameters</td>
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<td>(Continued on next page)</td>
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<tr>
<td>05/07/04</td>
<td>2.3</td>
<td>• Section &quot;DC Characteristics Over Operating Conditions,&quot; page 26:</td>
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<tr>
<td>(cont'd)</td>
<td></td>
<td>♦ Added parameter row and parameters for parallel configuration mode, 'P' devices, to ICCO, I_CCINTs, ICCOS, and ICCJS, to define active and standby mode requirements.</td>
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<td>(cont'd)</td>
<td></td>
<td>• Section &quot;AC Characteristics Over Operating Conditions,&quot; page 27:</td>
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<tr>
<td></td>
<td></td>
<td>♦ Corrected description for second T_CAC parameter line to show parameters for 1.8V VCCO.</td>
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<td></td>
<td>♦ Revised Footnote (7) to indicate VCCO = 3.3V.</td>
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<tr>
<td></td>
<td></td>
<td>♦ Applied Footnote (7) to second T_CYC parameter line.</td>
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<tr>
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<td></td>
<td>• Section &quot;AC Characteristics Over Operating Conditions When Cascading,&quot; page 36: Revised Footnote (5) T_CYC Min and T_CAC Min formulas.</td>
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<tr>
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<td>• Table 14, page 39:</td>
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<td></td>
<td>♦ Added additional state conditions to CLK description.</td>
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<td></td>
<td></td>
<td>♦ Added function of resetting the internal address counter to CF description.</td>
</tr>
</tbody>
</table>
07/20/04 2.4  • Added Pb-free package options VOG20, FSG48, and VOG48.
  • Figure 6, page 14, and Figure 7, page 15: Corrected connection name for FPGA DOUT
    (OPTIONAL Daisy-chained Slave FPGAs with different configurations) from DOUT to DIN.
  • Section "Absolute Maximum Ratings," page 24: Removed parameter T_SOL from table. (T_SOL
    information can be found in Package User Guide.)
  • Table 2, page 3: Removed reference to XC2VP125 FPGA.

10/18/04 2.5  • Table 1, page 1: Broke out V_CCO / V_CCG into two separate columns.
  • Table 9, page 7: Added clarification of ID code die revision bits.
  • Table 10, page 8: Deleted T_CKMIN2 (bypass mode) and renamed T_CKMIN1 to T_CKMIN.
  • Table "Recommended Operating Conditions," page 25: Separated V_CCO and V_CCG parameters.
  • Table "DC Characteristics Over Operating Conditions," page 26:
    • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
    • Added Footnote (1) to I_CCO specifying no-load conditions.
  • Table "AC Characteristics Over Operating Conditions," page 27:
    • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
    • Expanded Footnote (1) to include XCF08P, XCF16P, XCF32P devices.
    • Added Footnote (8) through (11) relating to CLKOUT conditions for various parameters.
    • Added rows to T_CYC specifying parameters for parallel mode.
    • Added rows specifying parameters with decompression for T_CLKO, T_COH, T_FF, T_SF.
    • Added T_DDC (setup time with decompression).
  • Table "AC Characteristics Over Operating Conditions When Cascading," page 36:
    • Added most parameter values for XCF08P, XCF16P, XCF32P devices.
    • Separated Footnote (5) into Footnotes (5) and (6) to specify different derivations of T_CYC,
      depending on whether dual-purpose configuration pins persist as configuration pins, or
      become general I/O pins after configuration.

03/14/05 2.6  • Added Virtex-4 LX/FX/SX configuration data to Table 2.
  • Corrected Virtex-II configuration data in Table 2.
  • Corrected Virtex-II Pro configuration data in Table 2.
  • Added Spartan-3L configuration data to Table 2.
  • Added Spartan-3E configuration data to Table 2.
  • Paragraph added to FPGA Master SelectMAP (Parallel) Mode (1), Page 11.
  • Changes to DC Characteristics
    • T_OER changed, Page 26.
    • I_O changed for V_OI, Page 26.
    • V_CCO added to test conditions for IIL, I_LP, I_HP, and IIH, Page 26. Values modified for I_ILP and
      I_HP.
  • Changes to AC Characteristics
    • T_LC and T_HC modified for 1.8V, Page 31.
    • New rows added for T_CE and T_DEC, Page 30.
    • Minor changes to grammar and punctuation.
    • Added explanation of "Preliminary" to DC and AC Electrical Characteristics.

07/11/05 2.7  • Move from "Preliminary" to "Product Specification"
  • Corrections to Virtex-4 configuration bitstream values
  • Minor changes to Figure 7, page 15, Figure 12, page 20, Figure 13, page 21, and Figure 16, page 41
  • Change to "Internal Oscillator," page 8 description
  • Change to "CLKOUT," page 8 description
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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</table>
| 12/29/05   | 2.8     | - Update to the first paragraph of "IEEE 1149.1 Boundary-Scan (JTAG)," page 5.  
- Added JTAG cautionary note to Page 5.  
- Corrected logic values for Erase/Program (ER/PROG) Status field, IR[4], listed under "XCFxxP Instruction Register (16 bits wide)," page 6.  
- Sections "XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source," page 27, "XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source," page 30 and "XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source," page 33 added to "AC Characteristics Over Operating Conditions," page 27.  
- Notes for Figure 6, page 14, Figure 7, page 15, Figure 8, page 16, Figure 9, page 17, Figure 10, page 18, Figure 11, page 19, Figure 12, page 20, and Figure 13, page 21 updated to specify the need for a pull-up resistor if CF is not connected to PROGB.  
- Figure 4 and Figure 5 renamed to Table 7, page 6 and Table 8, page 6 respectively. All tables, figures, and table and figure references renumber this point forward.  
- Value for "ICCINT," page 26 updated from 5mA to 1mA for XCFxxP.  
- Block diagram in Figure 2, page 2 updated to show clock source muxing and route clocking to all functional blocks. |
| 05/09/06   | 2.9     | - Added Virtex-5 LX support to Table 2, page 3.  
- "VIL" maximum for 2.5V operation in "Recommended Operating Conditions," page 25 updated to match LVCMOS25 standard. |