**TTL AND-GATE MoHAT PROJECT**  
**EE 307, Spring 2006**

**Introduction:**

In fall quarter, 2005, Dr. Braun issued a two-fold challenge to his EE 307 students: to repair the AND-Gate shown in Figure P4.23 of Gopalan’s *Introduction to Digital Microelectronic Circuits*, and to improve the version of the same gate given in Gopalan’s errata. Building on student’s prior work, we offer further improvements to both circuits. Specifically, our group adjusted the values of various resistors to restore functionality to the first gate and optimise the figures of merit of both gates. Interested in seeing the fruits of our labour? Read on!

**Part 1a: A Malfunctioning AND-Gate**

**MODEL:**

**Figure P4.23 from Introduction to Digital Microelectronic Circuits**

![TTL AND-GATE Diagram](image)

The gate shown in Figure P4.23 looks normal, but some analysis and a PSpice simulation clearly illustrate that the circuit does not perform an AND function.
HYPOTHESIS:  Q₁ Reverse Active  
Q₂ Saturation  
Q₃ Saturation  
Q₄ Cut-Off  
Q₅ Saturation

ANALYSIS:  
A & B = 5V  
\( V_{B5} = V_{BE(SAT)5} = 0.8V \)  
\( V_{E3} = V_{B5} = 0.8V \)  
\( V_{B3} = V_{C2} = V_{E3} + V_{BE(SAT)3} = 0.8V + 0.8V = 1.6V \)  
\( V_{B2} = V_{C1} = V_{E3} + V_{BC(ON)2} = 1.6V + 0.7V = 2.3V \)  
\( V_{E2} = V_{C2} - V_{CE(SAT)2} = 1.6V - 0.1V = 1.5V \)  
\( V_{B1} = V_{C1} + V_{B(ON)1} = 2.3V + 0.7V = 3.0V \)  
\( V_{C3} = V_{E3} + V_{CE(SAT)3} = 0.8V + 0.1V = 0.9V \)  
\( I_{RB} = I_{B1} = (V_{CC} - V_{B1}) / R_{B} = (5.0V - 3.0V) / 4KΩ = 0.5mA \)  
\( I_{C1} = I_{C2} = I_{E1} + I_{B1} = 0.5mA + 0.1mA = 0.6mA \)  
\( I_{E2} = V_{E2} / R_{4} = 1.5V / 800Ω = 1.875mA \)  
\( I_{C2} = I_{E2} - I_{B2} = 1.875mA - 0.6mA = 1.275mA \)  
\( I_{R3} = I_{C3} = (V_{CC} - V_{C3}) / R_{3} = (5.0V - 0.9V) / 1.6KΩ = 2.5625mA \)  
\( I_{R2} = (V_{CC} - V_{B3}) / R_{2} = (5.0V - 1.6V) / 2KΩ = 1.7mA \)  
\( I_{B3} = I_{R2} - I_{C2} = 1.7mA - 1.275mA = 0.425mA \)  
\( 0.425mA + 2.5625mA + 0.425mA = 2.9875mA \)  
\( I_{R5} = V_{B5} / R_{5} = 0.8V / 1KΩ = 0.8mA \)  
\( I_{B5} = I_{E3} - I_{R5} = 2.9875mA - 0.8mA = 2.1875mA \)  
\( P = V_{CC} * I_{CC} \)  
P = \( V_{CC} * (I_{RB} + I_{R2} + I_{R3} + I_{RC}) \)  
\( I_{CC} = 0.5mA + 1.7mA + 2.5625mA + 0mA = 4.7625mA \)  
P = 5V * 4.7625mA = 23.8125mW

A=O, B=5V ; A=5V, B=0V ; A=B=0V  
\( V_{B5} = V_{BE(SAT)5} = 0.8V \)  
\( V_{E3} = V_{B5} = 0.8V \)  
\( V_{B3} = V_{C2} = V_{E3} + V_{BE(SAT)3} = 0.8V + 0.8V = 1.6V \)  
\( V_{C3} = V_{E3} + V_{CE(SAT)3} = 0.8V + 0.1V = 0.9V \)  
\( V_{B1} = V_{BE(SAT)} = 0.8V \)  
\( V_{C1} = V_{B2} = V_{CE(SAT)1} = 0.1V \)  
\( I_{RB} = I_{B1} = (V_{CC} - V_{B1}) / R_{B} = (5.0V - 0.8V) / 4KΩ = 1.05mA \)  
\( I_{R3} = I_{C3} = (V_{CC} - V_{C3}) / R_{3} = (5.0V - 0.9V) / 1.6KΩ = 2.5625mA \)  
\( I_{R2} = (V_{CC} - V_{B3}) / R_{2} = (5.0V - 1.6V) / 2KΩ = 1.7mA \)  
\( I_{B3} = I_{R2} - I_{C2} = 1.7mA - 1.275mA = 0.425mA \)  
\( I_{E3} = I_{C3} + I_{B3} = 2.5625mA + 1.7mA = 4.2625mA \)  
\( I_{R5} = V_{B5} / R_{5} = 0.8V / 1KΩ = 0.8mA \)  
\( I_{B5} = I_{E3} - I_{R5} = 4.2625mA \)
\[ P = V_{CC} * I_{CC} \]
\[ P = V_{CC} * (I_{RB} + I_{R2} + I_{R3} + I_{RC}) \]
\[ I_{CC} = 1.05mA + 1.7mA + 2.5625mA + 0mA = 5.3125mA \]
\[ P = 5V * 5.3125mA = 26.5625Mw \]

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**TEST:**
* FAULTY TTL AND Gate Gopalan Figure P4.23

Vcc 1 0 5V
VA 2 0 pulse(0 5 0 1ns 1ns 10us 20us)
VB 3 0 pulse(0 5 0 1ns 1ns 5us 10us)
RB 1 4 4k
R2 1 7 2k
R3 1 9 1.6k
RC 1 10 130
R4 6 0 800
R5 8 0 1k
CL 12 0 15pF
Q1A 5 4 2 NPNT
Q1B 5 4 3 NPNT
Q2 7 5 6 NPNT
Q3 9 7 8 NPNT
Q4 10 9 11 NPNT
Q5 12 8 0 NPNT
* C B E (Collector Base Emitter)
D1 11 12 SW

.MODEL NPNT NPN (TF=1E-10 TR=1E-8 CJE=0.5P + CJC=0.5P RC=5 BF=50 BR=0.2)
.MODEL SW D(IS=1E-14 TT=1E-10 RS=10 CJO=2P + VJ=0.7)
.TRAN 0 40us
.PROBE
.END
As the PSpice simulation indicates, the output voltage, V(12), is stuck, maintaining a more or less constant value regardless of input conditions. Having clearly identified the problem, we could begin to solve the problem.

After reviewing the work done by groups from Fall 2005, we decided to lower the value of the 800-Ω resistor to 400-Ω, thus repairing the gate. We began to tinker with a simulation of a working AND-Gate in order to maximize its Figure of Merit (FOM).
Part 1b: ENHANCED TTL AND-GATE WITH ADJUSTED VALUES

Before attempting to optimize the FOM of the repaired AND-Gate, we needed to make some assumptions. Although Dr. Braun did not specify any maximum values of gate delay, we wanted to produce a working AND-Gate that designers could utilize in a wide variety of real-world applications. Therefore, we imposed the following constraint on our design:

In order to market the corrected gate to the widest possible spectrum of users, we kept the delay time less than 12% of the period of the Least Significant Bit.

MODEL:
**HYPOTHESIS:**
- Q1 Reverse Active
- Q2 Saturation
- Q3 Saturation
- Q4 Cut-Off
- Q5 Edge Of Conduction

**ANALYSIS:**

**A=B=5V**

\[ V_{B5} = V_{BE(EOC)} = 0.6V = V_{E3} \]
\[ V_{B3} = V_{C2} = V_{E3} + V_{BE(SAT)} = 0.6V + 0.8V = 1.4V \]
\[ V_{B2} = V_{C1} = V_{C2} + V_{BC(SAT)} = 1.4V + 0.7V = 2.1V \]
\[ V_{B1} = V_{C1} + V_{BC(RA)} = 2.1V + 0.7V = 2.8V \]
\[ I_{B1} = (V_{CC} - V_{B1}) / 2K\Omega = (5V - 2.8V) / 2K\Omega = 1.1mA \]
\[ I_{C1} = I_{B2} = (\beta_{R} + 1) \times I_{B1} = 1.32mA \]
\[ V_{E2} = V_{C2} - V_{CE(SAT)} = 1.3V \]
\[ I_{E2} = V_{E2} / 400\Omega = 1.3V / 400\Omega = 3.25mA \]
\[ I_{C2} = I_{E2} - I_{B2} = 0.48mA \]
\[ I_{R2} = (V_{CC} - V_{C2}) / 2K\Omega = (5V - 1.4V) / 2K\Omega = 1.8mA \]
\[ I_{B3} = I_{R2} - I_{C2} = 1.8mA - 0.48mA = 1.32mA \]
\[ V_{C3} = V_{B3} - V_{BC(SAT)} = 1.4V - 0.7V = 0.7V \]
\[ I_{R3} = (V_{CC} - V_{C3}) / 1.6K\Omega = (5V - 0.7V) / 1.6K\Omega = 2.69mA \]

\[ P = V_{CC} \times I_{CC} \]
\[ P = V_{CC} \times (I_{RB} + I_{R2} + I_{R3} + I_{RC}) \]
\[ I_{CC} = 1.1mA + 1.8mA + 2.69mA + 0mA = 5.59mA \]
\[ P = 5V \times 5.59mA = 27.95mW \]

**A=B=0V ; A=0V, B=5V ; A=5V, B=0V**

\[ V_{B5} = V_{BE(EOC)} = 0.6V = V_{E3} \]
\[ V_{B3} = V_{C2} = V_{E3} + V_{BE(SAT)} = 0.6V + 0.8V = 1.4V \]
\[ V_{B2} = V_{C1} = V_{C2} + V_{BC(SAT)} = 1.4V + 0.7V = 2.1V \]
\[ V_{B1} = V_{C1} + V_{BC(RA)} = 2.1V + 0.7V = 2.8V \]
\[ I_{B1} = (V_{CC} - V_{B1}) / 2K\Omega = (5V - 2.8V) / 2K\Omega = 1.1mA \]
\[ I_{C1} = I_{B2} = (\beta_{R} + 1) \times I_{B1} = 1.32mA \]
\[ V_{E2} = V_{C2} - V_{CE(SAT)} = 1.3V \]
\[ I_{E2} = V_{E2} / 400\Omega = 1.3V / 400\Omega = 3.25mA \]
\[ I_{C2} = I_{E2} - I_{B2} = 0.48mA \]
\[ I_{R2} = (V_{CC} - V_{C2}) / 2K\Omega = (5V - 1.4V) / 2K\Omega = 1.8mA \]
\[ I_{B3} = I_{R2} - I_{C2} = 1.8mA - 0.48mA = 1.32mA \]
\[ V_{C3} = V_{B3} - V_{BC(SAT)} = 1.4V - 0.7V = 0.7V \]
\[ I_{C3} = (V_{CC} - V_{C3}) / 1.6K\Omega = (5V - 0.7V) / 1.6K\Omega = 2.69mA \]
\[ P = V_{CC} \times I_{CC} \]
\[ P = V_{CC} \times (I_{B1} + I_{C3}) \]
\[ I_{CC} = 1.1\text{mA} + 2.69\text{mA} = 3.79\text{mA} \]
\[ P = 5\text{V} \times 3.79\text{mA} = 18.95\text{mW} \]

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**TEST:**
* Enhanced TTL AND-Gate Gopalan Figure P4.23

Vcc 1 0 5V
VA 2 0 pulse(0 5 0 .01ns .01ns 500ns 1000ns)
VB 3 0 pulse(0 5 0 .01ns .01ns 250ns 500ns)
* VA 2 0 pulse(0 5 0 1ns 1ns 10us 20us)
* VB 3 0 pulse(0 5 0 1ns 1ns 5us 10us)

RB 1 4 2k
R2 1 7 2k
R3 1 9 1.6k
RC 1 10 100
R4 6 0 400
R5 8 0 1k
CL 12 0 15pF
Q1A 5 4 2 NPNT
Q1B 5 4 3 NPNT
Q2 7 5 6 NPNT
Q3 9 7 8 NPNT
Q4 10 9 11 NPNT
Q5 12 8 0 NPNT
* C B E (Collector Base Emitter)
D1 11 12 SW

.MODEL NPNT NPN (TF=1E-10 TR=1E-8 CJE=0.5P + CJC=0.5P RC=5 BF=50 BR=0.2)
.MODEL SW D(IS=1E-14 TT=1E-10 RS=10 CJO=2P + VJ=0.7)

.TRAN 0 4000ns
.PROBE
Simulating this circuit in PSpice shows that it now produces the desired AND function. The Figure of Merit calculations follow:

Tested @ 2MHz
Delay = 7.425ns
Area = 710 µm²

\[
\text{FOM (Figure of Merit)} = \frac{(\text{delay in ns}) \times (\text{power in W}) \times (\text{area in } \mu\text{m}²)}{(\text{Freq. in GHz})}
\]

\[
= (7.425) \times (.02795) \times (710) / (.002)
\]

\[
= 71,168.625
\]
Part 2a: Gopalan’s Repaired AND-Gate

In his errata to the text, Gopalan provides his own corrected version of the AND-Gate analyzed in part 1 above. We will verify that this gate operates correctly by hand analysis and PSpice simulation. Then, we offer our own version of the gate with resistance values adjusted in order to optimize the gate’s Figure of Merit.

MODEL:

![AND-Gate Diagram]

Figure 4.23 from Gopalan Errata, with unmodified resistors

HYPOTHESIS:

Q1  Saturated
Q2  Off
Q3  Off
Q4  Saturated
Q5  Off
Q6  Saturated
ANALYSIS:

\[ V_{B2} = V_{in} + V_{CE1(sat)} = 0 + .1 = 0.1 \text{ V} \]
\[ I_{B4} = (V_{DD} - (V_{D1(on)} + V_{BE4(sat)} + V_{BE6(sat)}))/2k = (5 - (0.7 + .8 + .8))/2k = 1.35 \text{ mA} \]
\[ V_{B5} = V_{C4} = V_{BE6(sat)} + V_{CE4(sat)} = 0.8 + 0.1 = 0.9 \text{ V} \]
\[ V_{E5} = V_{CEE(sat)} + V_{D1(almost on)} = 0.1 + 0.5 = 0.6 \text{ V} \]
\[ V_{BE5} = V_{B5} - V_{E5} = 0.9 - 0.6 = 0.3 \text{ V} \]
\[ I_{C4} = (V_{DD} - V_{C4})/1.6k = (5 - 0.9)/1.6 = 2.56 \text{ mA} \]
\[ I_{E4} = I_{B4} + I_{C4} = 1.35 + 2.56 = 3.91 \text{ mA} \]
\[ V_{B6} = V_{BE(sat)} = 0.8 \text{ V} \]
\[ I_{B1} = (V_{DD} - V_{B1}) / 4k = (5 - .8)/4k = 1.05 \text{ mA} \]
\[ I_{C6} = 0 \text{ mA} \]
\[ V_{out} = V_{CE6(sat)} = 0.1 \text{ V} \]
\[ P_{D} = (V_{DD})(I_{B1} + I_{B4} + I_{C4}) = (5V)(1.05mA + 1.35mA + 2.56mA) = 24.8 \text{ mW} \]

HYPOTHESIS:

Q1 Reverse Active
Q2 Saturated
Q3 Forward Active
Q4 Off
Q5 Edge Of Conduction
Q6 Off

ANALYSIS:

\[ V_{B2} = V_{BE3(on)} + V_{BE2(sat)} = 0.7 + 0.8 = 1.5 \text{ V} \]
\[ V_{B1} = V_{B2} + V_{BC1(on)} = 1.5 + 0.7 = 2.2 \text{ V} \]
\[ I_{B1} = (V_{DD} - (V_{B2} + V_{BC1(on)}))/4k = (5 - (1.5 + 0.7))/4k = 0.7 \text{ mA} \]
\[ I_{C1} = I_{B2} = (BR + 1) I_{B1} \]
\[ I_{C1} = 0.7 * (1 + .2) = I_{B2} = 0.84 \text{ mA} \]
\[ V_{C2} = V_{BE3(on)} + V_{CE2(sat)} = 0.7 + 0.1 = 0.8 \text{ V} \]
\[ V_{C1} = V_{B2} = 1.5 \text{ V} \]
\[ I_{C2} = (V_{DD} - V_{C})/2k - I_{C3} \]
\[ I_{C3} = B_{F} I_{B3} \]
\[ I_{E3} = (V_{E2} / .8k) + I_{B3} = (V_{BE(on)}/ .8k) + I_{B3} \]
\[ V_{BE(on)} = 0.7 \text{ V} \]
\[ I_{E3} = (0.875 \text{ mA}) + I_{B3} \]
\[ I_{B3} = (0.84 \text{mA} + 2.1 \text{mA} - 0.875 \text{mA}) / (B_F + 1) \]
\[ I_{B3} = 0.041 \text{ mA} \]
\[ I_{E3} = B_F I_{B3} = 50 \times 0.041 \text{mA} = 2.0245 \text{ mA} \]
\[ I_{E2} = I_{B3} + I_{C2} \]
\[ I_{E2} = 0.041 \text{mA} + 0.875 \text{mA} = 0.92 \text{mA} \]
\[ I_{C2} = I_{E2} - I_{B2} = 0.92 \text{mA} - 0.84 \text{mA} = 0.076 \text{mA} \]
\[ I_{B4} = (V_{DD} - V_{CE2(sat)} - V_{BE3(on)}) / 2k = (5 -.1 - .7) / 2k = 2.1 \text{ mA} \]
\[ V_{B4} = (V_{BE3(on)} + V_{CE2(sat)}) - V_{D2(on)} = (0.7 + 0.1) - 0.7 = 0.1 \text{V} \]

\[ V_{out} = V_{DD} - (V_{D(almost on)} + V_{BE5(eoc)}) = 5 - (0.5 + 0.6) = 3.9 \text{ V} \]
\[ P_D = (V_{DD})(I_{B4} + I_{B1}) = (5V)(2.1mA + .7mA) = 14 \text{ mW} \]

**TEST:**

* P4.23 Gopalan Revised TTL AND Gate Errata
* Erik Toraason, Nitin Singh, Eric Montany, Neil
* EE 307 Prof. Braun

VCC 13 8 5
VA 0 8 pulse(0 5 0 1ps 1ps 10us 20us)
VB 1 8 pulse(0 5 0 1ps 1ps 5us 10us)
R1 13 10 4k
R2 13 3 2k
R3 13 6 1.6k
R4 13 10 130
R5 4 8 800
R6 7 8 1K
Q1A 2 9 0 NPNT
Q1B 2 9 1 NPNT
Q2 3 2 4 NPNT
Q3 5 4 0 NPNT
Q4 6 5 7 NPNT
Q5 10 6 11 NPNT
Q6 12 7 8 NPNT
* C B E (Collector Base Emitter)
D1 5 7 DIODE
D2 11 12 DIODE
CL 12 0 15pF

.MODEL DIODE D(IS=1E-14 TT=1E-11 RS=10 CJO=2P VJ=0.7)
.MODEL NPNT NPN(TF=1E-10 TR=1E-8 CJE=0.5P CJC=0.5P RC=5 BF=50 BR=0.2)

.TRAN 0 40us
.PROBE
.END
Thus, Gopalan has corrected his version of the AND-Gate in the errata. In order to further enhance the performance of the gate, we now attempted to optimize its Figure of Merit. Our work follows in the next section: Enhanced TTL AND-Gate from Errata.
Part 2b: Enhanced TTL AND-Gate from Errata

Before attempting to optimize the FOM of this AND-Gate, we again had to make some assumptions. Wanting to produce a working AND-Gate that designers could utilize in a wide variety of real-world applications, we imposed the same constraint on this AND-Gate as the previous one.

In order to market the corrected gate to the widest possible spectrum of users, we kept the delay time less than 12% of the period of the Least Significant Bit.

**MODEL:**

![Figure 4.23 from Gopalan's errata with modified resistor values](image)

**Hypothesis:**

A Or B = 0V

Q1  Saturated
Q2  Off
Q3  Off
Q4  Saturated
Q5 Off
Q6 Saturated

**Analysis:**

\[ V_{B2} = V_{in} + V_{CE1(sat)} = 0 + .1 = 0.1 \text{ V} \]
\[ I_{B4} = (V_{DD} - (V_{D1(on)} + V_{BE4(sat)} + V_{BE6(sat)}))/3k = (5 - (0.7 + .8 + .8))/3k = .9 \text{ mA} \]
\[ V_{B5} = V_{C4} = V_{BE6(sat)} + V_{CE4(sat)} = 0.8 + 0.1 = 0.9 \text{ V} \]
\[ V_{E5} = V_{CE6(sat)} + V_{D1(almost \, on)} = 0.1 + 0.5 = 0.6 \text{ V} \]
\[ V_{BE5} = V_{B5} - V_{E5} = 0.9 - 0.6 = 0.3 \text{ V} \]
\[ I_{C4} = (V_{DD} - V_{C4})/1.6k = (5 - 0.9)/1.6 = 2.56 \text{ mA} \]
\[ I_{E4} = I_{B4} + I_{C4} = 1.35 + 2.56 = 3.91 \text{ mA} \]
\[ V_{B6} = V_{BE(sat)} = 0.8 \text{ V} \]
\[ I_{B1} = (V_{DD} - V_{B1}) / 5k = (5 - .8)/5k = .84 \text{ mA} \]
\[ I_{C6} = 0 \text{ mA} \]

\[ V_{out} = V_{CE6(sat)} = 0.1 \text{ V} \]
\[ P_D = (V_{DD})(I_{B1} + I_{B4} + I_{C4}) = (5V)(.84mA + .9mA + 2.56mA) = 21.5 \text{ mW} \]

**HYPOTHESIS:**

A & B = 5V:

Q1 Reverse Active
Q2 Saturated
Q3 Forward Active
Q4 Off
Q5 Edge Of Conduction
Q6 Off

**ANALYSIS:**

\[ V_{B2} = V_{BE3(on)} + V_{BE2(sat)} = 0.7 + 0.8 = 1.5 \text{ V} \]
\[ V_{B1} = V_{B2} + V_{BC1(on)} = 1.5 + 0.7 = 2.2 \text{ V} \]
\[ I_{B1} = (V_{DD} - (V_{B2} + V_{BC1(on)})) / 5k = (5 - (1.5 + 0.7)) / 5k = 0.56 \text{ mA} \]
\[ I_{C1} = I_{B2} = (B_R + 1) I_{B1} \]
\[ I_{C1} = 0.7 * (1 + .2) = I_{B2} = 0.84 \text{ mA} \]
\[ V_{C2} = V_{BE3(on)} + V_{CE2(sat)} = 0.7 + 0.1 = 0.8 \text{ V} \]
\[ V_{C1} = V_{B2} = 1.5 \text{ V} \]
\[ I_{C2} = (V_{DD} - V_{C})/3k - I_{C3} \]
\[ I_{C3} = B_F I_{B3} \]
\[ I_{E3} = (V_{E2} / 1k) + I_{B3} = (V_{BE(on)} / 1k) + I_{B3} \]
\[ I_{E3} = (0.7 \text{ mA}) + I_{B3} \]
\[ I_{B3} = (0.84mA + 2.1mA - .56mA) / (B_F + 1) \]
\[ I_{B3} = 0.047 \text{ mA} \]
\[ I_{E3} = .92mA \]
$I_{C3} = B_F I_{B3} = 50 \times 0.047\text{mA} = 2.35\text{mA}$

$I_{E2} = I_{B3} + I_{C2}$

$I_{E2} = 0.047\text{mA} + 0.56\text{mA} = 0.61\text{mA}$

$I_{C2} = I_{E2} - I_{B2} = 0.92\text{mA} - 0.84\text{mA} = 0.076\text{mA}$

$I_{B4} = (V_{DD} - V_{CE2(sat)} - V_{BE3(on)}) / 3k = (5 - 0.1 - 0.7) / 3k = 1.4\text{mA}$

$V_{B4} = (V_{BE3(on)} + V_{CE2(sat)}) - V_{D2(on)} = (0.7 + 0.1) - 0.7 = 0.1\text{V}$

$V_{out} = V_{DD} - (V_{D(almost\ on)} + V_{BE5(eoc)}) = 5 - (0.5 + 0.6) = 3.9\text{V}$

$P_D = (V_{DD})(I_{B4} + I_{B1}) = (5\text{V})(1.4\text{mA} + .56\text{mA}) = 9.8\text{Mw}$
**TEST:**

* EE 307 Project
* TTL AND from Errata

Vcc 1 0 5V

VA 2 0 pulse(0 5 0 .01ns .01ns 125ns 250ns)
VB 3 0 pulse(0 5 0 .01ns .01ns 62.5ns 125ns)

RB 1 4 5k
R2 1 7 3k
R3 1 9 1.6k
RC 1 13 150
R4 6 0 1k
R5 10 0 2k
CL 15 0 15pF

Q1A 5 4 2 NPNT
Q1B 5 4 3 NPNT
Q2 7 5 6 NPNT
Q3 8 6 0 NPNT
Q4 9 8 10 NPNT
Q5 13 9 14 NPNT
Q6 15 10 0 NPNT
* C B E (Collector Base Emitter)

D1 7 8 SW
D2 14 15 SW

.MODEL NPNT NPN (TF=1E-10 TR=1E-8 CJE=0.5P + CJC=0.5P RC=5)

.MODEL SW D(IS=1E-14 TT=1E-10 RS=10 CJO=2P + VJ=0.7)

.TRAN 0 20us
.PROBE
.END
Simulating this circuit in PSpice shows the performance of our enhanced gate. The Figure of Merit calculations follow:

Tested @ 8 MHz
Delay = 10.0 ns
Area = 1275 µm²

FOM (Figure of Merit) = (delay in ns) x (power in W) x (area in µm²) / (Freq. in GHz)
= (10.0) x (.0260) x (1275) / (.008)
= 33,150.0
**Conclusion:**

In the analysis outlined in this report, we have attempted to improve on two AND-Gates given in Gopalan’s textbook *Introduction to Digital Microelectronic Circuits*. Specifically, we optimized each gate’s Figure of Merit by using the MoHAT (Model, Hypothesize, Analyze, Test) technique as demonstrated in Dr. Braun’s EE 307 class. Dr. Braun limited our modifications to changing resistance values in the circuits shown.

Because Dr. Braun made no mention of minimum or maximum allowable gate delays, we – a team of engineers – attempted to create a design that other engineers could utilize in a wide variety of real-world applications. To do this, we maximized both gate’s Figure of Merit while keeping the gate delay time less than 12% of the period of the Least Significant Bit.