Spartan 3 Brief Overview

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<table>
<thead>
<tr>
<th>Device</th>
<th>System Gates</th>
<th>Equivalent Logic Cells</th>
<th>CLB Array (One CLB = Four Slices)</th>
<th>Distributed RAM Bits (K=1024)</th>
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<th>Dedicated Multipliers</th>
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<th>Maximum User I/O</th>
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</tr>
</thead>
<tbody>
<tr>
<td>XC3S50</td>
<td>50K</td>
<td>1,728</td>
<td>Rows 16, Columns 12, Total 192</td>
<td>12K</td>
<td>72K</td>
<td>4</td>
<td>2</td>
<td>124</td>
<td>56</td>
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<td>XC3S200</td>
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<td>4,320</td>
<td>Rows 24, Columns 20, Total 480</td>
<td>30K</td>
<td>218K</td>
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<td>56K</td>
<td>288K</td>
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<td>XC3S1000</td>
<td>1M</td>
<td>17,280</td>
<td>Rows 48, Columns 40, Total 1,920</td>
<td>120K</td>
<td>432K</td>
<td>24</td>
<td>4</td>
<td>391</td>
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<td>XC3S1500</td>
<td>1.5M</td>
<td>29,952</td>
<td>Rows 64, Columns 52, Total 3,328</td>
<td>208K</td>
<td>576K</td>
<td>32</td>
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<td>XC3S2000</td>
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<td>46,080</td>
<td>Rows 80, Columns 64, Total 5,120</td>
<td>320K</td>
<td>720K</td>
<td>40</td>
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<td>565</td>
<td>270</td>
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<tr>
<td>XC3S4000</td>
<td>4M</td>
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<td>Rows 96, Columns 72, Total 6,912</td>
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<td>1,728K</td>
<td>96</td>
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<td>712</td>
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<tr>
<td>XC3S5000</td>
<td>5M</td>
<td>74,880</td>
<td>Rows 104, Columns 80, Total 8,320</td>
<td>520K</td>
<td>1,872K</td>
<td>104</td>
<td>4</td>
<td>784</td>
<td>344</td>
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</table>

Notes:
1. Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
2. These devices are available in Xilinx Automotive versions as described in DS314: Spartan-3 Automotive XA FPGA Family.

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Notes:
1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

Figure 1: Spartan-3 Family Architecture
Figure 3: Spartan-3 BGA Package Marking Example for Part Number XC3S1000-4FT256C
Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

Figure 5: Simplified IOB Diagram
Figure 9: Arrangement of Slices within the CLB
Notes:
1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. In this position, the upper right-hand slice has an F3MUX, and the upper left-hand slice has an F7MUX. The lower right-hand and left-hand slices both have an F5MUX.

Figure 10 Simplified Diagram of the Left-Hand SLICEM
Figure 11: Block RAM Data Paths
Figure 16: Embedded Multiplier Primitives
Figure 22: Spartan-3 Clock Network (Top View)
Figure 23: Types of Interconnect