Review for Final: CPE 329 Fall 2007

- Lectures 1-14, Therac-25, Chapters 1 & 2, Labs 1-5
- Exam Review Outlines
- Homework problems
- ISE/EDK technology
- Digilent Nexys board and peripherals technology
  - Not held accountable for specifics of Digilent D2FT-DIO5 technology, just principles
- No coding, just pseudo code (no syntax)
- One page (both sides) of reference notes
- Calculator
Exam Review Outline: lecture 1

CPE 329 Overview

• Course Description
• Course Learning Objectives
• Topics Covered
• Prerequisite material
• Course Material
• Lab Overview
  – Development Environment (CAD Tools)
  – Lab Equipment
    – Processor
• Lab Experiments
  – Experiment 1 Hardware-Based Digital Clock
  – Experiment 2 MicroBlaze “Hello World!”
  – Experiment 3 Microcontroller-Based Digital Clock
  – Experiment 4 Function Generator
  – Experiment 5 Final Design Project
Exam Review Outline: lecture 2
Introduction to Digital Systems

- **Taxonomy of Digital Systems**
  - Advantages and Disadvantages of each category (Cost, performance, ease of design, customization, configurability, integration, number of transistors)

- **Semiconductor Technology Trends**
  - Moore’s Law Number of transistors per die doubles every couple of years (historical data)
  - ITRS Future Projection
  - Increase in the number of practicing engineers per year
  - Must work at higher levels of abstraction
    - Increasing levels of abstraction for HW and SW
  - Hardware Software Co-design
Exam Review Outline – lecture 3

Programmable Logic

• History of Integrated Circuits
• Advantages of CPLDs
• Programmable Elements to connect nets or configure hardware devices
  - One-time-programmable (OTP) – Fuse/Antifuse
  - Re-programmable
    • Volatile (SRAM)
    • Non-Volatile (EEPROM, Flash)
• CPLD Architecture Functional Blocks
  - SPLD like configurable logic
    • MacroCell
    • MacroBlock
  - Programmable Interconnect
  - I/O Blocks
• FPGA Architecture
  - FPGA Fabric
    • Configurable Logic Block (Programmable MUX, Look Up Table, Pass Transistor)
    • Programmable Interconnect
    • I/O Blocks
    • Block RAM Memory
    • Hardcore blocks (ie Multipliers, PowerPC)
  - System on Chip (Soc) using Hardcore or Softcore Processors
Exam Review Outline

- **Programmable Interconnect (6-transistor junction)**
  - Direct – CLB to CLB
  - Local
  - Global
  - Timing - Clock networks

- **Propagation delay timing for interconnect 1st order model**
  - Wired interconnect $t_{PLH}$
  - Programmable interconnect $t_{PLH}$

- **Design Example of 8-bit Ripple Carry Adder**
  - CPLD Design
    - Full Adder
  - FPGA Design
    - 2-bit adder subcomponent
    - LUT programming (Combining LUTs for more input variables)
    - Programmable interconnect
  - Adder Using VHDL
Exam Review Outline

- **Design Flow**
  - Designer
    - Write HDL Code
    - Simulate
    - Constraints
  - CAD Tool
    - Synthesis
    - Translate/Map
    - Place and Route
    - Generate Programming File
    - Download bit file
- **Xilinx FPGA and CPLD**
  - Spartan IIE FPGA Architecture
    - FPGA Fabric
    - I/O Block
    - CLB and CLB Slice
    - Product Family
  - CoolRunner XPLA3 Architecture
    - Features
    - Architecture Block Diagram
    - PLA Logic Inputs
    - Logic Block (MacroBlock)
    - I/O Cell
    - MacroCell
    - Timing Model
- **Xilinx Spartan 3 – Nexys Board**
Exam Review Outline – lecture 4
Embedded Systems and MicroBlaze Computer System

- Computer Systems, Processors, and Terminology
  - Custom HW - ASIC, VLSI, ...
  - Processor vs. Microprocessor
  - Microcomputer vs. Microcontroller
  - Embedded system design process
    - Requirements
    - Specifications
    - Architecture
    - Components
    - System Integration
  - Embedded System
    - Characteristics: Complex Algorithms, user interface, real-time, multi-rate
    - Costs: Cost of goods, mfg cost, development cost
    - Challenges
      - Hardware performance vs. Cost
      - Code Space/ Code Density
      - Need to meet real-time demands
      - Minimize power consumption
      - Design for upgrade-ability
      - Verification
      - Reliability
Exam Review Outline

- **Embedded Systems Continued**
  - Computer System Block Diagram
  - System on Chip - SoC
    - Processor in ASIC or FPGA with Softcore processor
  - Programmers model - Registers, Condition Codes and Instruction Set Architecture
  - Why is it important to know ISA?
  - Computer Classification
    - Architecture
      - Von Neuman / Princeton Architecture
      - Harvard Architecture
      - DSP’s
    - RISC vs. CISC

- **EDK computer system**
  - MicroBlaze Processor
  - Busses (ILMB, DLMB, IOPB and DOPB)
  - MicroBlaze Memory System
    - Memory Controllers and BRAM
  - Memory Mapped I/O
  - IP Cores
  - GPIO Programming Input and Output Devices
Exam Review Outline

- Base Address
- Memory Mapped Registers (Data Register and Data Direction Register)
- I/O Instructions
  - Software functions to read and write MicroBlaze memory locations
    - `Xio_In32();` and `Xio_Out32();`
    - `xparameters.h` and `xio.h`
  - DIO5 I/O Controller
    - Bus Based Interface Between FPGA and I/O Controller
    - Computer System
      - Bus Write Cycle
        - Timing Diagram
        - Algorithm to implement using GPIO and MicroBlaze
  - DIO5 Memory Map of I/O Devices
  - LCD initialization Routine
  - LCD Display Characters
  - Nexys interface to LCD and peripherals (buttons and leds)
Exam Review Outline – lecture 5
Xilinx Embedded Developers Kit

- Embedded Developers Kit Design Flow
  - Hardware System
    - Add Cores
    - Bus Connection
    - Memory Map
    - Port Connections
    - Parameters
    - User Constraints
  - Software System
    - Device Driver Interface (Xio_Out, Xio_In, …)
    - Main Code using “C”
    - Compile
    - Generate Bitstream
    - Update Bitstream
    - Download code
Exam Review Outline – lecture 6

MicroBlaze Instruction set, Architecture, Performance, and Interrupts

- **MicroBlaze**
  - Programmers Model
  - Data Types
  - Instruction Set
  - Program Counter and Machine State Register
  - General Purpose Registers
  - Instruction formats

- **Big Endian / Little Endian**

- **Pipelining**
  - Overlapped execution
  - Performance (Latency, throughput, IPC, and CPI)
  - MicroBlaze Pipeline (F->D->Execute)
  - Data Dependency Hazards
  - Control Hazards
  - Delayed Branches
Timers and Counters

Interrupts
- Asynchronous event that allows device to interrupt CPU and transfer control over to an interrupt service routine.
- Foreground task (main loop)
- Interrupt Service Routing (ISR) or Interrupt Handler
- Interrupt and Acknowledge
- Hardware interface for interrupt
- Interrupt process at HW level
  - CPU initializes and enables interrupt device and unmasks interrupts
  - External Interrupt request generated
    - Possibly on chip peripheral device
    - Possibly external device
  - CPU typically finishes current instruction
    - Some instructions are interruptible
  - Some CPU’s perform HW context save (if not context save is responsibility of ISR)
  - CPU’s typically disable interrupts automatically
  - Return address stored (on stack or in dedicated register)
  - Branch to interrupt service routine: Fetch Interrupt Vector (address of interrupt service routine) or address of instruction in jump table and put this address into the PC
  - Execute the interrupt service routine
  - ISR must clear interrupt flag (acknowledge interrupt)
  - Restore Context if not handled in HW
  - RTI - Return from interrupt instruction: Restores CPU context including condition codes and Branches to return address

- Debugging with interrupts
- Multiple Interrupts and Interrupt Priorities
- Maskable vs. Non-Maskable interrupts
- Handling multiple interrupts using an OR gate
- Interrupt controllers and multiple interrupt devices
- Interrupt overhead
- Comparison of Interrupts to Polling algorithms
Exam Review Outline – lecture 8
Digital-to-Analog Conversion and Analog-to-Digital Conversion

• Sampling theory
  – Sampling Frequency
  – Resolution

• Analog-to-Digital Converters
  – Sample and Hold
  – Summing op-amp circuit

• Digital-to-Analog Converters
  – Analog Devices AD7303 Architecture
  – AD7303 IP Core and device drivers
  – Software for digital-to-analog conversion
  – Digilent AIO1 Interface Board setup and schematic

• Interfacing Sensors
  – Resolution and Selection of $V_{REF}$
  – ADC digital output
  – LM35 Temperature Sensor
Exam Review Outline – lecture 9
Serial I/O and Programming Input and Output

- Data Management
  - FIFO
  - Stack
  - Software Implementation of FIFOs and Stacks
- I/O Algorithms for UART with Keyboard and Monitor Algorithm
  - I/O with busy waiting and Memory Mapped I/O
    - How it works
    - Algorithm (flow chart)
    - C code implementation
  - I/O with interrupts
    - I/O Buffer Queue
      - With separate input and output device interrupt handlers that can run at different speeds we need a place to store incoming data.
      - FIFO or circular queue
      - Head and tail pointers
      - Storing and removing characters
      - Queue empty, queue full, number of characters in queue
    - How it works
    - Algorithm (flow chart)
    - C code implementation
  - Task processing with ISRs
Exam Review Outline – lecture 10
Other I/O Devices

- Switches and Pushbuttons to digital logic (circuit and resistance)
- Debouncing Switches and Pushbuttons
  - SR latch
  - RC filter
  - Software Debounce algorithm
- Keypad
  - Direct wired keypad
  - Matrix keypad
    - Operation
    - benefit
- Keyboard
- PC Keyboard (microcontroller, serial interface, scan codes)
  - PS2 port
  - Bidirectional Clock and data
  - Master Slave
  - Communication with Keyboard and Host
  - Timing diagram
- Scanned Keyboard: Benefits and Issues
- Mouse
  - Unidirectional
  - Timing diagram
- Touch-screen Displays
  - Vertical and Horizontal Position
Exam Review Outline

- LEDs
- I-V Characteristics
- Circuit and current limiting resistor
- 7-Segment Displays
  - 7-segment code
  - Circuit elements
  - Raster scan
- Cathode Ray Tube (CRT)
- Directly driven (Data, Horizontal and Vertical Deflection)
- Frame buffer device driver
- VGA Controller
  - Interface/Connector
  - Video RAM
- Character LCD Displays
  - Controller and LCD
  - Addressing Modes
  - ASCII Characters
  - DRAM Buffer
  - Font Table
  - Hardware interface
- Graphical LCD Displays
  - Pixel by Pixel Control RGB
Exam Review Outline – lecture 11

Other Peripheral Devices: External Memory controller and Serial Peripheral Interfaces

• External memory controllers
  - SRAM structure
  - SRAM memory block – data-in and data-out busses, bidirectional data bus
  - Memory read and write signals – proper assertion of control signals
  - OPB EMC core
    • Parameter configuration
    • Register model
    • Timing of read and write cycles

• Serial peripheral Interface
  - Four concepts: Serial, synchronous, Master-slave protocol, data exchange
  - IO signals
  - Master-slave configuration
  - SPI mode
    • Clock polarity
    • Clock phase
  - OPB SPI core
    • SCK, slave select, MOSI, MISO signals
    • Register model
Exam Review Outline – lecture 12

Power Consumption and Energy

- Heat Generation depends on Power Consumption
- Battery Life depends on Energy Consumption
- In CMOS what causes power consumption
  - Static
    - Leakage Current
    - Sub Threshold Current
    - Passive Current dissipation
  - Dynamic
    - Switching Current
    - Charging and Discharging Capacitive loads
- \[ P_{\text{cap}} = \alpha C_{\text{eff}} V_{\text{dd}}^2 f, \quad E_{\text{cap}} = \alpha C_{\text{eff}} V_{\text{dd}}^2 \]
- Methods to Reduce Power and Energy Consumption
- Power management
  - Static
  - Dynamic
  - Power management state machines
  - StrongARM Example
Exam Review Outline – lecture 13

Survey of Microcontroller Market and Common Microcontrollers

• Microcontroller market segments
• Microcontrollers vs. Microprocessors
• Market analysis
• Alternate Microcontroller Devices
  – PIC
  – Atmel
  – Mot HC12
  – Mot 68000
• DSPs
  – Applications
  – What is a digital signal processor
  – TMS 320
  – DSP5600
Exam Review Outline – lecture 14
Ethics in Engineering

- IEEE Code of Ethics
- Engineering ethics issues
  - Cheating
  - Responsibility
  - Scapegoating
  - Intellectual Property
  - Whistle Blowing
  - Outsourcing
  - Layoffs
  - Engineering integrity
  - Conflict of interests
  - Gifts
  - Product Readiness
  - Discrimination
- Therac-25 Case
  - Players
  - Incidents
  - In-class group discussion
Laboratory Review

- Lab 1 Digital Clock Design Using Programmable Logic and VHDL
  - Nexys/ISE tutorial exp 0
  - Review of VHDL and Xilinx ISE, MicroSim
  - Digital clock requirements
  - Development process
  - Laboratory procedures
Laboratory Review

- Lab 2 MicroBlaze “Hello World” and Embedded Development Kit (EDK)
  - EDK 9.1i-nexys board tutorial
  - “C” programming review
  - GPIO
  - Interface to LCD
    - Documentation
    - Interface protocol
    - Timing diagram
Laboratory Review

- Lab 3 MicroBlaze Digital Clock and the Embedded Development Kit
  - Timer/counter peripheral
  - Interrupts
  - Nexys buttons
  - Use of LCD driver code
  - Demo: testing <-> specifications
Laboratory Review

- Lab 4 MicroBlaze Function Generator Design
  - SPI
  - PMOD DA2
  - Analog instrumentation for verification
  - Reuse of C code, peripherals
Laboratory Review

• Lab 5 Computer Application Final Design Project
  – Additional peripheral interface: ADC, PS/2
  – Additional interface protocols
  – Building on knowledge gained in previous labs
  – Demonstrate ability to find interface information
  – Hardware/software tradeoff in design
  – Minimal hardware/software resources
  – “C” coding style
  – Oral presentation
  – Proper embedded system project documentation