The purpose of these team PSpice projects are to introduce the student to the use of PSpice for the analysis of transmission lines, to use PSpice as a tool to learn the theory presented in lecture, and to analyze more complicated transmission line problems than pencil and paper conveniently allow, and to introduce the student to team project work. It is assumed that all students have used PSpice in previous classes, and have access to PSpice on a computer, either at home or at Cal Poly. The EE 335 class is to form into two or three person teams for the PSpice assignments; teams can be greater than three, but the larger teams will require the prior approval of the instructor. For the submittal of each assignment, each team will submit one report, with each team member providing one thoughtful, reflective paragraph discussing what they have learned.

You are required to find the step response of the following transmission line circuit for five different loads using a PSpice analysis:

a) matched 50 ohms
b) mismatched 10 ohms
c) open circuit
d) short circuit
e) parallel rc load with 50 ohms and 1 nF

The code for case e) is presented below; use this code as a template to simulate all the cases. For each case, provide a Probe plot of V(2), V(3), and V(4) as defined in the circuit below. Note that V(2) is the source input voltage for the TL, V(3) is similar to a time domain reflectometry response and represents a voltage at a location within the TL, and V(4) is the load voltage for the TL.

*ee 335 TDR TL tl_rc_tdr.cir
*parallel rc load 50 ohm and 1nF
vg 1 0 pulse(0 1 0 1ns 1ns .5us 1us) ; 0 to 1V pulse, zero delay, 1ns rise/fall time, 0.5us width, 1us period
rg 1 2 50
tl 2 0 3 0 z0=50 td=40n ; lossless TL: input 2 0, output 3 0, Zo=50 ohms, time delay 40us
t2 3 0 4 0 z0=50 td=40n ; lossless TL: input 2 0, output 3 0, Zo=50 ohms, time delay 40us
r1 4 0 50
c1 4 0 1n
.tran 0.1n 250n 0 1n ; transient analysis: print step, stop time, [optional parameters: start time, maximum internal step time]
.probe
.end

Note that by modifying the above template code that other cases can be analyzed, including circuits with lumped parameter models between the TLs and the TLs having different parameters for Zo and time delay. You are encouraged to explore these possibilities to observe the wave phenomena. Also, an analytical analysis of the parallel RC load case is available on the course website; see TL_notes_4-7-06. This PSpice project 1 is due Friday April 14.