**Purpose:** This project introduces the student to the time domain response of transmission lines. The effects of time (or propagation) delay caused by a transmission line to the step response of a five different loads will be investigated: matched, mismatched, open circuit, short circuit, and parallel RC. The results will be discussed in the context of the performance of practical digital circuits. The step response of each load will be investigated in three ways: using a simulation with PSpice, a mathematical analysis, and a measurement circuit. For each case, the results of each investigation will be compared.

**References:**
EE 402 Text  
Iskander, Magdy F.; Electromagnetic Fields and Waves; Waveland Press; 2000  
Chapter 7, especially sections 7.1-9

**Equipment:**
HP 3312 Function Generator  
Tektronix 2215 Oscilloscope  
1 16 meter RG 58/U cable  
3 short (around 30 cm) RG 58/U cables  
2 BNC Tees  
1 BNC to double banana adapter  
BNC-double banana: 50 ohm load resistor; 10 ohm resistor; open circuit; short circuit, parallel RC load (50 ohm and 160 pF)  
PSpice on workstation computer

**Discussion:**
In this experiment, we will use a technique first presented in your lower division circuits laboratory to observe the step response of a circuit. The technique is to use an appropriately chosen squarewave to periodically repeat a positive step input to a circuit. Note that a positive DC offset is applied to the squarewave so that the squarewave appears to just be a positive pulse. Then only the positive portion of the squarewave is observed; however, nothing prevents observation of the effects of the second half of the squarewave. The period $T$ of the squarewave is determined so that the step response of the circuit is essentially in steady state at a time $T/2$, i.e., half the period. This technique allows the periodic voltages observed with an oscilloscope to be the complete step response. The same basic technique is used to provide the input voltage waveform for a PSpice simulation (see the template code below).

The unique feature of this project is that with relatively inexpensive, low performance instrumentation and a long transmission line (16m), we can show the time domain effects of wave propagation, i.e., the step response of a circuit with propagation delay under different loading conditions. The observed voltages present the same phenomena as a practical circuit which has dimensions commensurate with the wavelength of its signals, $\dim = \frac{\lambda}{f}$, where $\dim$ is the dimension of the circuit, $\lambda$ is the wavelength in the media of the circuit, $v_p$ is the velocity of propagation in the media of the circuit, and $f$ is the frequency of the signal (volts). In this project the transmission line is an RG 58 A/U which has a velocity of propagation of about $2 \times 10^8$ m/s, which yields a propagation delay of about 80 ns for a 16m cable. Thus with the 60MHz scope and a 1 MHz squarewave function generator (and properly chosen values for the RC load to get a reasonable time constant), the effects of the propagation delay can be measured. Note that the characteristic impedance of the RG 58A/U is 50 ohms. The output impedance of the HP 3312A function generator also is 50 ohms, so the source (function generator) is matched to the transmission line. This follows because the small length of transmission line (about 30 cm) which connects the function generator to the oscilloscope also is RG 58 A/U and is matched to the source. The effect of the loading of the oscilloscope output impedance (parallel 1 Mohm and 14 pF) also is negligible as the time constant due to the output impedance and connecting transmission lines is estimated to be less than 1ns, and therefore too small to observe. The effect of the oscilloscope impedance can be simulated though.
Part I (Prelab): PSpice Simulation
Note: If you don't have a copy of PSpice, then you can obtain a CD at the senior project window in 20-111.
Using PSpice, simulate the following circuit for five cases using PROBE to display V(2) and V(3):
   a) 50 ohm matched load
   b) 10 ohm mismatched load
   c) open circuit
   d) short circuit
   e) parallel RC load (50 ohm and 160 pF)
For each case, provide a copy of the PROBE output for V(2) and V(3), and a one paragraph description of
why the waveform for V(2) has the shape presented in the simulation. Also, to prepare for the experiment
read the Part II (laboratory project), and in particular, review the Exp A Analysis notes. The Exp A
Analysis notes presents a mathematical model for the step response of the transmission line circuits that
students will be asked to use to predict and to understand the phenomena observed.

![Transmission Line Measurement Circuit](image)

Use the following template PSpice code to construct your simulation:

```
*ee 442 exp A time domain analysis tl rc
*parallel rc load 50 ohm and 160 pF
vg 1 0 pulse(0 1 0 1ns 1ns .5us 1us) ;0 to 1V pulse, 0 delay, 1ns rise/fall time, 0.5us width, 1us period
rg 1 2 50
tl 2 0 3 0 z0=50 td=80ns ;lossless TL: input 2 0, output 3 0, Zo=50ohms, time delay 80ns
rl 3 0 50
c1 3 0 160p ;transient analysis 0.1ns print step, 500 ns duration,
.tran 0.1n 500n 0 0.1n ;tstart=0 (initial print value), tmax=0.1 (max internal step size)
.probe
.end
```

Part II (laboratory project)

a) Matched 50 ohms Load:
   1. The simulation and analysis will now be verified with measurements. Construct the transmission line
circuit given in Figure 1. Use V(2) as the channel 1 input and trigger; connect the first Tee on the scope
channel 1 connection. Connect the banana load with 50 ohm resistor directly to the first Tee (no
transmission line), and observe the voltage V(2) for an input voltage of 1 MHz square wave with 1.0 Vpp
and +500mV DC offset. Provide a sketch of the voltage V(2).

   2. Connect the matched load with the 16 meter transmission line, and connect V(3) to channel 2 of the
scope (use the second Tee). Using the same input voltage, observe the voltages V(2) and V(3) for each
case. Provide sketches of the voltages V(2) and V(3) on the same figure.

   3. Use the analytic form presented in the analysis to provide sketches for the voltages V(2) and V(3).
   Compare the results of the simulation, analysis, and measurement; how close are they?
Discussion: Notice that with a matched load, the reflection coefficient of the load $\Gamma_L = 0$, and the value of the reflected (negative going) wave is zero. However, the delay observed can have a deleterious effect on the performance of a synchronous (clocked) digital circuit. The delay in the signal can impact the satisfaction of the set-up time requirement for flip-flops. Variable delays caused by different length signal traces can cause clock skew, where the edge of a clock waveform will occur at different times for different flip-flops. Also, the maximum delay limits the minimum clock period that can be used, i.e., the period must be larger than the maximum delay for correct synchronous signal interpretation.

b) Mismatched 10 ohms Load:
1. Connect the banana load with 10 ohm resistor directly to the first Tee (no transmission line), and observe the voltage $V(2)$ for the same source voltage. Provide a sketch of the voltage $V(2)$.

2. Connect the mismatched load with the 16 meter transmission line, and connect $V(3)$ to channel 2 of the scope (use the second Tee). Using the same input voltage, observe the voltages $V(2)$ and $V(3)$ for each case. Provide sketches of the voltages $V(2)$ and $V(3)$ on the same figure.

3. Use the analytic form presented in the analysis to provide sketches for the voltages $V(2)$ and $V(3)$. Compare the results of the simulation, analysis, and measurement; how close are they?

Discussion: Notice that with a mismatched load, the reflection coefficient of the load $\Gamma_L = -0.66$, and the value of the amplitude of the reflected (negative going) wave is -0.66. Now there is not only a delay in the response for $V(3)$ at the load, but there is a reflected wave that affects the $V(2)$ waveform at the source. Hence, the waveform voltage at $V(2)$ does not remain constant after the reflected wave arrives, has another value (what is it?). Note that this case is only an example of a mismatch load, and that other values of a load resistance not equal to $Z_0$ will cause different values for $V(2)$ in the steady state. This change could affect the interpretation of the digital logic level at the source and at the load, and hence give rise to improper circuit performance.

c) Open Circuit Load
1. Connect the open circuit load directly to the first Tee (no transmission line), and observe the voltage $V(2)$ for the same source voltage. Provide a sketch of the voltage $V(2)$.

2. Connect the open circuit load with the 16 meter transmission line, and connect $V(3)$ to channel 2 of the scope (use the second Tee). Using the same input voltage, observe the voltages $V(2)$ and $V(3)$ for each case. Provide sketches of the voltages $V(2)$ and $V(3)$ on the same figure.

3. Use the analytic form presented in the analysis to provide sketches for the voltages $V(2)$ and $V(3)$. Compare the results of the simulation, analysis, and measurement; how close are they?

Discussion: The open circuit load shows the effect of a time delay of about 80 ns. The initial $V(2)$ is the positive going wave only. The change in the value of voltage at the load demonstrates the creation of the negative going wave; note that $\Gamma_L = 1$, i.e., the positive and negative voltage wave are equal. Notice what happens at the source after the reflected wave arrives. At this point in time, the transmission line is in steady-state, i.e., it has a constant voltage. On a printed circuit board, the effect observed can be caused by a trace that is not connected, leading to spurious values. However, the effect can be used to advantage; the PCI bus interface used in PCs uses an open circuit at each end of the bus to increase the voltage level of the signal lines through the use of the reflected wave from the open circuits.

d) Short Circuit Load
1. Connect the short circuit load directly to the first Tee (no transmission line), and observe the voltage $V(2)$ for the same source voltage. Provide a sketch of the voltage $V(2)$.

2. Connect the short circuit load with the 16 meter transmission line, and connect $V(3)$ to channel 2 of the scope (use the second Tee). Using the same input voltage, observe the voltages $V(2)$ and $V(3)$ for each case. Provide sketches of the voltages $V(2)$ and $V(3)$ on the same figure.
3. Use the analytic form presented in the analysis to provide sketches for the voltages V(2) and V(3). Compare the results of the simulation, analysis, and measurement; how close are they?

Discussion: Notice the delay in obtaining a value of the voltage at the source of 0V; again, there is a transient response before the steady-state values are observed for the transmission line. A PCB trace which is shorted to ground will have the same behavior. The reflection coefficient of the load is \( \Gamma_L = -1 \), i.e., the negative voltage wave is the negative of the positive voltage wave. This leads to the steady-state value of current (short circuit current) which is limited by the value of the function generator output impedance which is 50 ohms and which is matched with the characteristic impedance of the transmission line, \( Z_0 = 50 \) ohms.

e) Parallel RC load

1. Connect the banana parallel RC load with 50 ohm and 160 pF directly to the first Tee (no transmission line), and observe the voltage V(2) for the same source voltage. Note that the load resistor is matched to \( Z_0 \) and the time constant is much less than the transmission line delay. Provide a sketch of the voltage V(2).

2. Connect the parallel RC load with the 16 meter transmission line, and connect V(3) to channel 2 of the scope (use the second Tee). Using the same input voltage, observe the voltages V(2) and V(3) for each case. Provide sketches of the voltages V(2) and V(3) on the same figure.

3. Use the analytic form presented in the analysis to provide sketches for the voltages V(2) and V(3). Compare the results of the simulation, analysis, and measurement; how close are they?

Discussion: The parallel RC load is a model for a matched load which has a parasitic capacitance connected in parallel to it. All connections (nodes) on a PCB comprise a two conductor system, which is a capacitor; a typical rule of thumb is that there are 1 pF at every node due to this effect. This intrinsic parasitic capacitance effect is a fundamental limitation for the input to any electronic circuit, and was recognized by Bode in the 1930’s. Notice that the load has the same voltage waveform whether it is connected to the transmission line or directly. For the case of this load, the analysis shows the form of the negative voltage wave, and its subsequent effect on the source voltage for this step response. The effect of the negative going wave on the source voltage is a glitch; after a delay, the voltage at the source goes briefly to zero, and then returns to the steady-state value for the transmission line. Obviously, this behavior in a digital circuit could cause erroneous results. The design of synchronous digital circuits address this possibility by specifying when signals are sampled, generally at the edge of a clock signal (which occurs only during a relatively short period of time) – it doesn't matter what the signal does at other times. Asynchronous circuits on the other hand have to deal with this problem in very clever ways.

Note: Don't forget to end your report with the individual thoughtful, reflective paragraphs discussing what has been learned from the experiment.
Step response of transmission line circuit with various loads.

\[ V_g(t) = u(t), \text{ step} \]

\[ R_g = 2 \alpha, \text{ matched source} \]

\[ T = \frac{k}{V_g}, \text{ propagation delay of TL} \]

\[ (1) \quad v_t(t) = u^+(t-\frac{3\alpha}{2}) + u^-(t+\frac{3\alpha}{2}) \]

TL at rest (no stored energy) \[ \Rightarrow v_t^+(t+\frac{3\alpha}{2}) = 0, \quad 0 \leq t \leq T \]

Applying boundary conditions at source to get \[ v_t^+(t-\frac{3\alpha}{2}) = u_v(t) \]

\[ u_v(t) = \frac{v_h(t)-v_q(t)}{R_g} = v_q(t) - v_h(t) \]

\[ \Rightarrow v_t^+(t) = \frac{2\alpha}{2\alpha+3\alpha} v_q(t) \text{ and with } R_g = 2\alpha \text{ and } v_q(t) = u(t) \]

\[ v_t^+(t) = u^+(t-\frac{3\alpha}{2}) = \frac{2\alpha}{2\alpha+3\alpha} u(t-\frac{3\alpha}{2}) = \frac{1}{2} u(t-\frac{3\alpha}{2}) \]

Apply boundary conditions for load

\[ v_h(t) = u(t), \quad v_q(t) = v^+(t) + v^-(t) \]

\[ i(t) = \frac{v(t)}{Z_0} = \frac{u(t)}{Z_0} \quad \Rightarrow Z_0 i(t) = u^+(t) - u^-(t) \]

Solving (1) and (2) for \[ u^+(t) \] by adding

\[ 2u^+(t) = v_h(t) + i(t)Z_0 \]

\[ u^+(t) = \frac{Z_0}{2Z_0} v_h(t) + \frac{Z_0}{2Z_0} i(t)Z_0 = \frac{1}{2} u(t+\frac{3\alpha}{2}) \quad \Rightarrow (3) \]

\[ u(t+\frac{3\alpha}{2}) = u^+(t) + i(t+\frac{3\alpha}{2})Z_0 \quad \text{note } Z_0 = Z_0 \quad \Rightarrow (4) \]

Since TL circuit is linear time invariant (LTI), we can solve for each load with input voltage \[ u(t) \], then shift solution by \( t \to t+\frac{3\alpha}{2} \) to get step response of load, i.e., \[ u^+(t) \to u^+(t) \]

a) matched load

\[ v(t) = v_h(t) \]

Substituting into (4), version of (4):

\[ v(t) = v_h(t) + \frac{Z_0}{2Z_0} i(t)Z_0 = v_h(t) + \frac{Z_0}{2Z_0} Z_0 = \frac{1}{2} v(t) \]

\[ i(t) = \frac{1}{2} u(t) \]

Using LTI principle, \[ u(t) = v_h(t-\frac{3\alpha}{2}) = \frac{1}{2} u(t-\frac{3\alpha}{2}) \text{ and by } (3) \]

\[ v(t) = u^+(t) + v^-(t) = \frac{1}{2} u(t-\frac{3\alpha}{2}) + u^+(t) = \frac{3}{2} u(t-\frac{3\alpha}{2}) \]
which yields \( V^{-}(t) = 0 \) for no reflected wave.

This gives:

\[
V(t^+ - \delta t) = V^{-}(t - \delta t) = \frac{1}{2} u(t^+ - \delta t)
\]

b) mismatched load.

\( V_{LH} = R_L \frac{u(t)}{R_L} \) and following case (a)

\[
\begin{align*}
V(t^+) &= \frac{R_L}{R_L + R_0} u(t^+) \\
V(t^-) &= \frac{R_L}{R_L + R_0} u(t^-) \\
\therefore \ u(t) &= \frac{R_L}{R_L + R_0} \left[ u(t^+) + u(t^-) \right] \\
\Rightarrow \ u(t) &= \frac{R_L}{R_L + R_0} \left[ \frac{R_L}{R_L + R_0} u(t) + \frac{R_L}{R_L + R_0} u(t) \right] \\
\text{note with}\ R_L > R_0, \ u(t) &= \frac{R_L}{R_L + R_0} u(t)
\end{align*}
\]

\( V(t) = \frac{R_L}{R_L + R_0} v(t) \)

\( u(t) = \frac{1}{2} \left[ u(t^+) + u(t^-) \right] = \frac{1}{3} \left[ u(t^+ + 2T) + u(t^- + 2T) \right] \)

\( i_L(t) = 0 \)

c) open circuit load.

\[
\begin{align*}
i_L(t) &= 0 \quad \text{and following case (a)} \quad \frac{d}{dt} i_L(t) = 0 \\
i_L(t) &= \frac{V_L(t)}{R_L} + 0 \delta t = \frac{V_L(t)}{R_L} \\
\therefore \ u(t) &= \frac{V_L(t)}{R_L} + v^-(t) \\
\Rightarrow \ u(t) &= \frac{1}{2} \left[ u(t^-) + v^-(t) \right] \quad \Rightarrow \quad u(t) = \frac{1}{2} \left[ u(t^-) + v^+(t) \right] \\
\text{and} \quad \frac{dv}{dt} = 0
\end{align*}
\]

\[
\begin{align*}
\Rightarrow \ u(t^+) &= \frac{1}{2} \left[ u(t^- + 2T) + v^+(t) \right] \\
\text{d) short circuit load.} \\
\therefore \ u(t) &= \frac{1}{2} \left[ u(t^- + 2T) + v^+(t) \right] \\
\text{and following case (a) again} \quad \frac{d}{dt} i_L(t) = 0 \\
i_L(t) &= \frac{V_L(t)}{R_L} + 0 \delta t = \frac{V_L(t)}{R_L} \\
\therefore \ i_L(t) &= \frac{V_L(t)}{R_L} \\
\Rightarrow \ u(t^-) &= \frac{V_L(t^-)}{R_L} = \left[ \left( I_L(t^-) = \frac{V_L(t^-)}{R_L} \right) \right] \\
\Rightarrow \ u(t) &= v^+(t) - v^-(t) \\
\Rightarrow \ u(t) &= -\frac{1}{2} \left[ u(t^-) + v^+(t) \right] \quad \text{and} \quad \frac{dv}{dt} = -1
\end{align*}
\]

\[
\begin{align*}
\Rightarrow \ u(t^-) &= \frac{1}{2} \left[ u(t^- - 2T) + v^+(t) \right] \\
\text{and following case (a) again} \quad \frac{d}{dt} i_L(t) = 0 \\
i_L(t) &= \frac{V_L(t)}{R_L} + 0 \delta t = \frac{V_L(t)}{R_L} \\
\therefore \ i_L(t) &= \frac{V_L(t)}{R_L} \\
\Rightarrow \ u(t^-) &= \frac{V_L(t^-)}{R_L} = \left[ \left( I_L(t^-) = \frac{V_L(t^-)}{R_L} \right) \right] \\
\Rightarrow \ u(t) &= v^+(t) - v^-(t) \\
\Rightarrow \ u(t) &= -\frac{1}{2} \left[ u(t^-) + v^+(t) \right] \quad \text{and} \quad \frac{dv}{dt} = -1
\end{align*}
\]
Parallel RC load

By KCL: \( \frac{dV(t)}{dt} + \frac{V(t)}{R} + \frac{V_2(t)}{R_2} = 0 \)

following case (a)

\( V(t) = V_{01}(t) + (t - 0) \frac{dV_{02}(t)}{dt} + \frac{V_{03}(t)}{R} \)

new assuming \( V(t) = 0 \), i.e., at rest, then solve diff eq. for \( t \geq 0 \)

3 homogeneous solution

\( 2c^2 + \frac{c}{R} + \frac{1}{R} \frac{dV_{02}(t)}{dt} = 0 \) \( \Rightarrow \frac{dV_{02}(t)}{dt} = \frac{2c}{R} e^{-ct} \)

\( \therefore \frac{dV_{02}(t)}{dt} = ke^{-ct} \) with \( \tau = \frac{R}{2c} \) \( \Rightarrow \frac{dV_{02}(t)}{dt} = \frac{ke^{-ct}}{2c} \)

2 particular solution

\( \frac{dV_{04}(t)}{dt} + \frac{c}{R} + \frac{1}{R} \frac{dV_{02}(t)}{dt} = 1 \) \( \forall t \geq 0 \)

using method of undetermined coefficients with \( V_{04}(t) = A \)

\( \frac{dV_{04}(t)}{dt} = A \) \( \forall t \geq 0 \)

\( \frac{dV_{04}(t)}{dt} = \frac{ke^{-ct}}{2c} \)

2 total

\( V(t) = V_{02}(t) + V_{04}(t) = ke^{-ct} + \frac{ke^{-ct}}{2c} \)

now \( V(t) = 0 \) \( \Rightarrow \frac{ke^{-ct}}{2c} \)

\( \therefore V(t) = \frac{ke^{-ct}}{2c} (1 + e^{-ct}) \) with \( \tau = \frac{R}{2c} \)

now \( V(t) = \frac{ke^{-ct}}{2c} (1 - e^{-ct}) \)

\( \therefore V(t) = \frac{ke^{-ct}}{2c} (1 - e^{-ct}) \) \( \forall t \geq 0 \)

\( \therefore V(t) = \frac{ke^{-ct}}{2c} (1 - e^{-ct}) \) \( \forall t \geq 0 \)

was is \( R_2 = R_0 \), e.g., matched resistor with parasitic capacitance

\( V(t) = \frac{ke^{-ct}}{2c} (1 - e^{-ct}) \) \( \forall t \geq 0 \)

again, note \( c = \frac{2c}{R_0} \) \( c = \frac{2c}{R_0} \) \( \Rightarrow \) \( \therefore \tau \leq \frac{T_0}{2} \) for steady-state