1. (10) State the five axioms and their duals that define the Boolean algebra \((2^1)\).

\[
\begin{align*}
\text{1. a. } x + 0 &= x &\quad \text{16. } x = 1 \lor x = 0 \\
\text{2. a. } x + 0 = x &\lor \text{16b. } x = 1 \lor x = 0 \\
\text{3. a. } 0 \cdot 0 &= 0 &\quad \text{3b. } 1 + 1 = 1 \\
\text{4. a. } 1 \cdot 1 &= 1 &\quad \text{4b. } 0 \cdot 0 = 0 \\
\text{5. a. } 0 \cdot 1 &= 1 \cdot 0 = 0 &\quad \text{5b. } 1 + 0 = 0 + 1 = 1
\end{align*}
\]

2. The following partial listing for VHDL code implements a frequency divider to create a synchronous clock, slo_clk, from the system clock, clk. In the code, the declaration for signal count uses \(n\) and the slo_clk signal uses \(k\) as variables for the purposes of this question. If the frequency of clk is 1024 Hz, then determine the frequency of slo_clk when:

```vhdl
architecture behavioral of problem2 is

    signal count: std_logic_vector (n downto 0);
    signal slo_clk: std_logic;

begin
    frequency-divider: process(clk)
    begin
        if rising_edge(clk) then count <= count + 1;
        end if;
        slo_clk <= count(k);
    end process;

a. (5) \(n = k = 6\).

\[
\begin{align*}
\frac{f_a}{f_b} &= \frac{f_{\text{clk}}}{2^m}, \text{ where } m = \text{number of bits} \\
\frac{f_a}{f_b} &= \frac{1024}{2^6} = \frac{2^{10}}{2^6} = 2^4 = 8 \text{ Hz} \\
\end{align*}
\]

b. (5) \(n = 5\) and \(k = 3\).

\[
\frac{f_b}{f_b} = \frac{1024}{2^{3+1}} = \frac{2^{10}}{2^4} = 2^6 = 64 \text{ Hz}
\]
3. Given the following logic diagram that realizes the logic function relating the output variable z to the input variables a, b, and c, then complete the template VHDL code for the architecture declaration using the dataflow style indicated. Add a comment to the entity code that defines the relationship between the logic vector f and the input variables a, b, and c for your answer.

--- note other solutions

library IEEE;
use IEEE.STD_LOGIC_1164.all;
~ =~ f(2) = a, f(1) = b, f(0) = c
entity prob3 is port (
    f: in std_logic_vector (2 downto 0);
    z: out std_logic
);
end prob3;

a.(10) simple signal assignment (Boolean equations)

architecture dataflow of prob3 is
begin
    z <= (f(2) and f(1) and f(0)) or (not f(2) and f(1) and f(0))
end dataflow;

b.(10) conditional signal assignment (when-else statement)

architecture dataflow of prob3 is
begin
    z <= "1" when f = "111" else
        "1" when f = "011" else
        "0"
end dataflow;

c.(10) selected signal assignment (with-select-when statement)

architecture dataflow of prob3 is
begin
    with f select
    begin
        z <= "1" when "111";
        "1" when "011",
        "0" when others
    end
end dataflow;
4. (20) Given the template VHDL code, implement the synchronous finite state machine defined by the state diagram given below using the two process PS/NS method. Define any signals that are needed to complete your implementation.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity prob4 is port (
    x, clk: in std_logic;
    f: out std_logic
);
end prob4;

architecture behavior of prob4 is

    type state_type is (a, b);
    signal ps, ns : state_type;

begin
    sync_process : process (clk)
    begin
        if rising_edge(clk) then
            ps <= ns;
            if x = '1' then
                ps <= a;
            else
                ps <= b;
            end if;
        end if;
    end process sync_process;

    comb_process : process (ps, x)
    begin
        case ps is
            when a => f <= '1';
            when b => f <= '0';
            when others => f <= '0';
        end case;
    end process comb_process;
end behavior;
```

5. (10) The state diagram for a synchronous mealy finite state machine with the state variable q, the input x, and the output z is given below. Given the input x and that the initial state is q = 0 as shown and that the state changes on the rising edge of the clock, then complete the timing diagram for the variables q and z. For your solution, assume the propagation delays are negligible.
6.(10) The VHDL code for a clocked synchronous finite state machine is given below. Showing all work, determine the state diagram and state whether it is a mealy or moore machine.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity prob6 is port (  
    x, clk: in std_logic;
    z: out std_logic 
    );
end prob6;

architecture dataflow of prob5 is
    signal d: std_logic;
    signal q: std_logic;
begin
    d <= (not q) and x;
    z <= not q;
    q <= d when rising_edge(clk) else q;
end dataflow;
```

7.(10 @ 2) Provide a very brief answer to teach of the following questions; the objective is to assess that you know each of the concepts presented.

a) What are the names of the five components that constitute a computer?
   - Input, Output, Memory, Control (state machine), Data path/AW

b) What is the difference between a Harvard and a Princeton computer architecture?
   - Harvard has two memories: one for instruction and one for data

c) What are the four basic operations that constitute a computer machine cycle?
   - Fetch, decode, execute, write-back

d) What are the contents of the program counter of a computer?
   - Address of next instruction

e) What is metastability in a logic circuit?
   - Instability in the response of a clocked synchronous circuit due to an asynchronous input (violation of setup/hold times)