The exam will be closed book, but students will be provided a VHDL reference sheet with the exam (same as exam 1). It will cover chapters 1-9 of the reader, homework 1-7, all labs thru expc7, and the lecture material presented in class. In addition, students will be held accountable for the prerequisite material in CPE 129/169, as noted in the exam 1 review and this review. The knowledge in this course is cumulative, and the exam 1 review should be reviewed also. Again, note that as part of the exam, each student is expected to sign the following statement: “I have neither been given nor have received during this exam unauthorized assistance per the university policy on cheating.”

Material in review for exam 1

Emphasis for exam 2:

truth table <-> logic function <-> logic diagram <-> VHDL

{state diagram <-> state/output table <-> timing diagram} <-> logic diagram <-> VHDL

assembly language programming:
  use of EASY1 for VBC1
  programmer’s register model (PRM) for EASY1
  instructions <-> transfer function form using micro operations (register transfer language)
  concept of macro, e.g., subtraction with addi, division with sro
  write assembly language programs for VBC1

computer components and their implementation (expc4-c7): data path units, instruction memory unit, monitor system, instruction decoder

use of timing diagrams to analyze logic design, combinational and sequential (state machines)
  concept of propagation delay for gates and flip-flops
  setup and hold times for flip-flops
  estimation of critical path propagation delay for logic circuit
  estimation of maximum clock frequency of operation
  concept of safety margin