The exam will be closed book and notes, and no calculator. A summary sheet for VHDL will be provided with the exam, and a copy can be found at the course website for review before the exam. Bring a pencil and eraser, all paper will be provided. The final exam will cover all the material in the CPE 229/269 Reader; all homework 1-9, all labs expr thru expec9, and all the lecture material presented in class. In addition, students will be held accountable for the prerequisite material in CPE 129/169, as noted in the exam 1 review. The knowledge in this course is cumulative, and the exam 1 and 2 reviews should be reviewed also. Again, note that as part of the exam, each student is expected to sign the following statement: “I have neither been given nor have received during this exam unauthorized assistance per the university policy on cheating.”

Exam 1 Review

Exam 2 Review

Skills and knowledge that the students are expected to know after taking this class for CPE 229/269:

Analyze a logic circuit (combinational, sequential or state machine) to determine what it does: combinational - truth table or logic function; sequential or state machine - state diagram or state output table; simulation with timing diagram.

Design a logic circuit from the following description: truth table, logic function, state diagram, state/output table, timing diagram (with discussion).

Given a logical word problem, translate it into a Boolean logic problem and design a logic circuit to implement its solution or code it in VHDL.

Understand the VBC1/EASY1 computer system, and be able to implement any given function in VHDL given sufficient discussion to define the question, e.g., concept of OUT data path and its control signals, concept of PC and JNZ data path, etc.

Understand the development of a relatively complex system (VBC1 on the order of 300-400 lines of VHDL code with comments) via a systematic process (documentation style M) with build-in test and diagnostic functions implicitly implemented with that process.

Ability to trouble-shoot and debug a relatively complex system (VBC1) as it is being developed.

Ability to work efficiently, effectively, and productively as a member of a two (or three) person development team satisfying specified requirements for that development.

Analysis of logic circuits to determine maximum propagation delay and hence maximum operating frequency

Ability to program in the VBC1 assembly language and simulate with EASY1

Ability to analyze a VHDL source to determine the logic circuit it implements in enough detail to fix any errors in coding if present.

Ability to implement a logic circuit or a schematic diagram with VHDL in a number of coding styles, and with proper comments.

Procedures for using the Xilinx ISE development environment and for implementing a resulting design on the Digilent Nexys board.

Use of timing diagrams to simulate a design for testing.