I have neither been given nor have received during this exam unauthorized assistance per the university policy on cheating.

Signature

1. (10) State the five axioms and their duals that define the Boolean algebra ($2^1$).

1. a. $x = 0, 1, x \neq 1$

1. b. $x = 1, 1, x \neq 0$

2. a. $1 \cdot x = 0, \text{then } x = 1$

2. b. $1 \cdot x = 1, \text{then } x = 0$

3. a. $0 \cdot 0 = 0$

3. b. $1 + 1 = 1$

4. a. $1 \cdot 1 = 1$

4. b. $0 + 0 = 0$

5. a. $0, 1 = 1, 0 = 0$

5. b. $1 + 0 = 0 + 1 = 0$

2. (15) The state diagram for a synchronous Moore finite state machine with the state variable $q$, the input variable $x$, and the output $z$ is given below. Complete the following timing diagram for the given clock and input signals as shown; that is, draw the signals $q$ and $z$. The initial state is $q = 0$, and the state changes on the rising edge of the clock signal; there are negligible propagation delays.

![State Diagram](image)

![Timing Diagram](image)
3. The compressed truth table for the data path control signals for the two VBC1 instructions MOV and ADD are given below. For control signal M2:

<table>
<thead>
<tr>
<th>IR</th>
<th>M1 M2 M3 M4 M5 M6 LOAD_R0 LOAD_R1 LOAD_OP</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV R0,R0</td>
<td>0 0 0 0 0 0 1 0 0</td>
</tr>
<tr>
<td>MOV R0,R1</td>
<td>0 1 0 0 0 0 1 0 0</td>
</tr>
<tr>
<td>MOV R1,R0</td>
<td>0 0 0 0 0 0 0 1 0</td>
</tr>
<tr>
<td>MOV R1,R1</td>
<td>0 0 0 0 0 0 0 1 0</td>
</tr>
<tr>
<td>ADD R0,R0</td>
<td>0 0 1 0 0 0 1 0 0</td>
</tr>
<tr>
<td>ADD R0,R1</td>
<td>0 1 1 0 0 0 1 0 0</td>
</tr>
<tr>
<td>ADD R1,R0</td>
<td>0 1 1 0 0 0 0 1 0</td>
</tr>
<tr>
<td>ADD R1,R1</td>
<td>0 1 1 1 0 0 0 1 0</td>
</tr>
</tbody>
</table>

a) (10) Determine a Boolean function for the control signal M2.

\[ M_2 = \overline{R(7)} \cdot \overline{R(6)} \cdot \overline{R(5)} \cdot \overline{R(3)} + \overline{R(7)} \cdot \overline{R(6)} \cdot \overline{R(5)} \cdot \overline{R(4)} \]

b) (5) Write a VHDL conditional signal assignment for the control signal M2.

\[ M_2 \leftarrow \begin{cases} R(3) \text{ when } \overline{R(7 \text{ downto } 5)} = \text{"000"} & \text{else} \\ \overline{R(4)} \text{ when } \overline{R(7 \text{ downto } 5)} = \text{"010"} & \text{else} \\ 0 & \end{cases} \]

4. (15) Given the following logic circuit with the following timing specifications:

- D flip-flops: setup time = 5 ns, hold time = 4 ns and output propagation delay = 15 ns = \( t_{Dpd} \)
- Gates: propagation delay = 10 ns, = \( t_{gpd} \)

Determine the maximum frequency that the circuit can operate properly. You must show all work and state all assumptions to get full credit.

- select critical path (longest total delay)

\[ (t_{delay})_{critical} = (10ns) + (10ns) + (10ns) + (15ns) + (15ns) \]

\[ (t_{delay})_{critical} = 50 \text{ ns} \]

\[ f_{max} = \frac{1}{(t_{delay})_{critical}} = \frac{1}{50\text{ ns}} = 20\times10^6 \text{ } \text{Hz} = 20 \text{ MHz} \]
5. (20 @ 2) Provide a very brief answer to each of the following questions; the objective is to assess that you know each of the concepts presented.

a) What are the names of the five components that constitute a computer?

input, output, memory, datapath/alu, control (state machine)

b) What is the difference between a Harvard and a Princeton computer architecture?

Harvard has separate memory for data and instructions.

c) Given that the 16 by 8 bit set of registers is the instruction memory, what are the names of the other six registers that constitute the programmer's register model for the VBC1 as used in EASY1?

input, output, PC, R1, R0, R1

d) What does the program counter do?

contain address of next instruction to execute

e) What is metastability in a logic circuit?

oscillations caused by asynchronous input to synchronous circuit

f) What function does a debouncing circuit perform?

allows single response from an input switch

g) What is the function of an assembler macro instruction?

allows a sequence of machine code to be referenced

h) If a system clock frequency is 10 MHz and a 2-bit counter is used to divide the frequency, what is the lowest frequency that can be generated for the 2-bit register?

\[ f_{10M} = \frac{10 \text{ MHz}}{2^2} = 2.5 \text{ MHz} \]

i) What are the four basic operations that constitute a computer machine cycle?

fetch, decode, execute, write back

j) What is the basic architectural difference between CISC and RISC computers?

RISC computer has much fewer machine instructions
6. Write an assembly language program with comments for the VBC1 using its eight instructions to perform the following algorithms. The first and last line of your program is given below; the other instructions and comments are to be determined by you. To be unambiguous in your written answer, use O = letter O and 0 = number zero. Remember that your program is limited to 16 machine code entries.

a)(10) Perform the arithmetic calculation: \( y = ((5 + 4) - 3)/2 \) where 5 is entered through the input port switches and 4 is entered via an instruction, i.e., immediate data, and the answer \( y \) is provided through the output port to the LEDs.

\[
\begin{align*}
\text{IN R0} & \quad ; \text{input the number 5 via the nexys switches sw3:sw0 = (1001)} \\
\text{ADDI R0,4} & \quad ; \text{add 4 to 5 in R0} \\
\text{ADDI R0,13} & \quad ; \text{2's complement for 3 as integer} \\
\text{SR R0,R0} & \quad ; \text{rotate right for divide by 2} \\
\text{MOV R1,R0} & \quad ; \text{move answer to R1 for output}
\end{align*}
\]

\[
\begin{align*}
\text{note:} & \quad 3 = 0011 \\
1's \text{ complement} & \rightarrow 1.100 \\
+1 & \quad 2's \text{ comp} = 1101 = 13_{10}
\end{align*}
\]

\[
\text{OUT R1} \quad ; \text{output answer y to ld3:ld0 = (0011)}
\]

b)(15) Perform the iterative sum: \( y = \Sigma 2 \), where the sum is from \( n=1 \) to 4, i.e.,

\[ y = 2+2+2+2 = 8. \]

The integer 2 is entered through the input port switches and the result \( y \) is provided through the output port to the LEDs. A loop using the JNZ instruction is required to be performed to implement the iterative sum.

\[
\begin{align*}
\text{IN R0} & \quad ; \text{input the number 2 via the nexys switches sw3:sw0 = (0010)} \\
\text{LOADI R1,3} & \quad ; \text{R1 contains loop variable (counter)} \\
\text{LOOP : ADDI R0,2} & \quad ; \text{perform first iteration} \\
\text{ADDI R0,15} & \quad ; \text{decrement loop counter R1} \\
\text{JNZ R0,LOOP} & \quad ; \text{check for end}
\end{align*}
\]

\[
\begin{align*}
\text{note:} & \quad 15 = 1111 \\
& \quad 2's \text{ complement of 0001}
\end{align*}
\]

\[
\begin{align*}
\text{OUT R0} & \quad ; \text{output answer y to ld3:ld0 = (1000)}
\end{align*}
\]