The exam will be open book (CPE 229/269 Reader only). It will cover chapters 1-4 of the reader; homework 1-3; labs expR and expC1-c3; and the lecture material presented in class. In addition, students will be held accountable for the prerequisite material in CPE 129, as noted in this review. Note that as part of the exam, each student is expected to sign the following statement: “I have neither been given nor have received during this exam unauthorized assistance per the university policy on cheating.”

Combinational Logic

Wakerly’s five axioms and their duals for Boolean algebra ($2^1$):

1a) $x = 0$, if $x != 1$
1b) $x = 1$, if $x != 0$
2a) if $x = 0$, then $!x = 1$
2b) if $x = 1$, then $!x = 0$
3a) $0 \cdot 0 = 0$
3b) $1 + 1 = 1$
4a) $1 \cdot 1 = 1$
4b) $0 + 0 = 0$
5a) $0 \cdot 1 = 1 \cdot 0 = 0$
5b) $1 + 0 = 0 + 1 = 1$

Concept of duality: {$\cdot, +, 0, 1$} $\leftrightarrow$ {$+, \cdot, 1, 0$}

Truth table $\leftrightarrow$ logic functions; use of POS and SOP

Use of truth table for proofs

deMorgan’s theorem: $!(x \cdot y) = !x + !y$

gates (not, and, or) to realize logic functions; symbols

functionally complete gates: nand, nor; realization of {not, and, or}; pushing bubbles thru

minimization of logic functions/gates to implement

adjacency theorem: $x \cdot y + !x \cdot y = y$; application to Karnaugh maps for minimization

timing diagrams and propagation delay

Sequential Logic

Latches and flip-flops: S-R, J-K, T and D; clock, SET, CLR, setup and hold times,

propagation delay, symbols

Next state, current state tables and characteristic equations

Realization of others by D

Finite State Machines: Mealy and Moore (“moore is less”) architecture

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X          Z=G(S,X) Mealy
\rightarrow S \rightarrow G \rightarrow memory \rightarrow F
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clocked synchronous state machines: analysis and design

design steps: problem statement $\rightarrow$ requirements $\rightarrow$ (specifications $\leftrightarrow$ testing)

state diagram $\leftrightarrow$ state/output table; issues of initial/power up state

state assignment (binary, one-hot, gray code); issue of unassigned states

transition/output table

transition equations

excitation equations (D flip-flop: $Q = D$)

output equations

logic diagram

note: analysis is the reverse order

propagation delay and estimate of maximum frequency of operation

Metastability and its prevention - synchronizers
Computer Architecture

Princeton (von Neumann) and Harvard architectures
computing process: fetch, decode, execute, write-back
instruction set architecture (ISA): CISC, RISC
programmer's register model (PRM)
assembly language and machine code

Introduction to very basic computer one (VBC1) and EASY1
Harvard architecture with 4-bit data/address paths and 8 8-bit instructions
Design overview
VBC1 machine code and assembly language
EASY1 PRM model for editing, assembly and simulation concepts

VHDL
Three parts: library, entity, architecture
Three styles of architecture: dataflow, behavioral, structural
Design of combinational logic with dataflow; conditional signal assignment (when-else), selected signal assignment (with-select-when (expc1))
Design of synchronous state machines with behavioral two process PS/NS: if-then and case (expc2 and expc3)